PRiME Research Brief

Power-efficient, Reliable, Many-core Embedded systems

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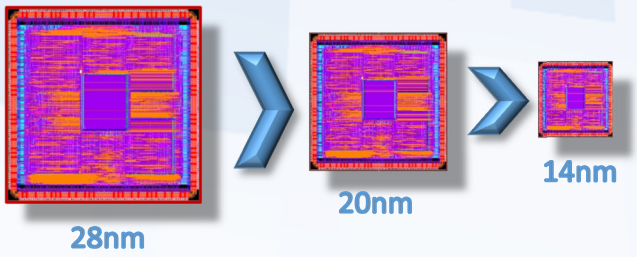
Using Online Timing Slack Sensors with DVFS to Reduce Timing Margins

*PRiME is a five year EPSRC funded research programme (2013-2018), in which four UK universities address the challenge of **power consumption** and **reliability** of future high-performance embedded systems utilising **many-core processors**.*

Process Technology Scaling

Scaling of the technology used to manufacture integrated circuits remains the driving force behind the semiconductor industry today, as manufacturers seek better power consumption, switching speed and transistor density.



As this continues, however, devices are increasingly experiencing the effect of *delay variability*, both at the time of manufacturing and during their operating lifetime, with increased susceptibility to changes in operating conditions. Newly manufactured devices experience delay variation of as much as ±15%, which can deteriorate by a further 20% during a 10 year operating life.

Chip manufacturers account for this variability by building in timing margins at the design/layout phase. As variability increases, so do these margins, eroding the benefit of technology scaling.

Online Timing Slack Measurement

Timing slack is the difference between the time that data is required, and the time it is provided. Timing slack is a good measure of circuit "health"; a large slack means that it would take a significant deterioration to cause timing issues, a small slack indicates that the circuit may be close to failure.

PRiME's **Online Timing Slack Measurement (OSM)** technology uses circuit-level sensors to directly quantify the timing slack at critical parts of an operating circuit. It can do so accurately and with a low area and performance overhead.

OSM has been demonstrated on Altera Cyclone III/IV FPGAs, and **PRiME** has developed tools that can automatically instrument arbitrary circuits implemented on these devices. We are currently working towards doing so for the new Cyclone and Stratix families.

Dynamic Voltage Frequency Scaling using OSM

Dynamic Voltage Frequency Scaling (DVFS) can alleviate some of the timing margins required to guarantee circuit operation under the effect of delay variation by using measurement information to control the operating parameters of the circuit. OSM provides direct measurement of timing slack in the operating circuit, avoiding the models required for indirect measurement techniques.

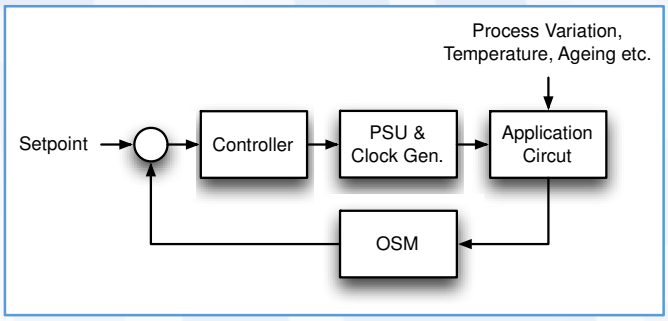


Figure 1. Block diagram of the DVFS controller

Figure 1 shows the DVFS controller. The instrumented application circuit is perturbed by delay variation, the effect of which is directly measured using OSM. The controller then compares the measured slack to a setpoint and controls the power supply and/or clock generator. This setpoint is a small timing margin that is maintained to allow for delay variability that cannot be accounted for - it is much smaller than that required without DVFS.

DVFS Control Modes

PRiME has developed three different scaling modes: frequency constrained, voltage constrained and power constrained. These constraints can be static, or interactive. When static, the constraint is kept constant, while in interactive case a higher-level runtime can vary the constraint during operation.

For example, in interactive frequency constrained control, the frequency is configured and the controller optimises the circuit's voltage. Power constrained DVFS controls both the voltage and frequency in order to maintain the power consumption within a specified envelope while maximizing throughput.

These six scaling modes can cater to real-time embedded systems, low-power embedded systems, high-performance systems and everything in between.

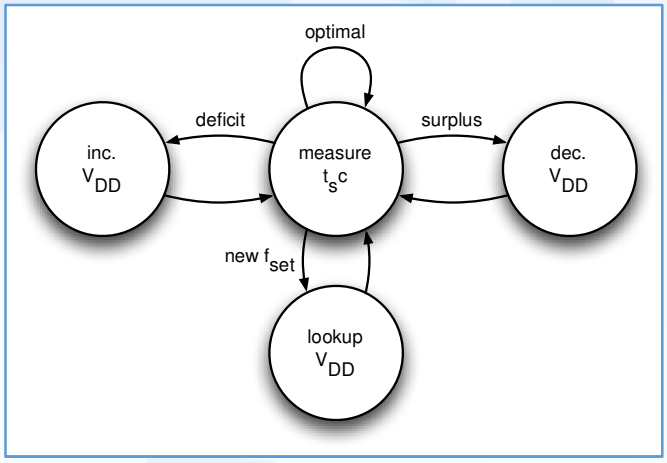


Figure 2. Diagram of the interactive frequency constrained DVFS controller

Figure 2 shows the interactive frequency constrained controller. This simple, stepping controller attempts to maintain an optimal timing margin slack by increasing the voltage if a slack deficit is measured (slack > setpoint timing margin), and decreasing if a surplus. When a new frequency is specified the controller looks up a safe operating voltage from a pre-characterised table and then fine grain closed-loop control resumes.

Results

Experiments have established the effectiveness of this DVFS approach. Benchmark circuits were automatically instrumented and run on an Altera Cyclone IV, with a temperature-controlled package, and performance parameters measured.

Figure 3 shows the power consumption of the nominal circuits (unscaled and at nominal voltage and timing mode fmax) as compared to static frequency constrained DVFS at room temperature and 85℃ (the upper temperature corner). An average power reduction of 25% is achieved at 85℃, this increases to 34% at room temperature.

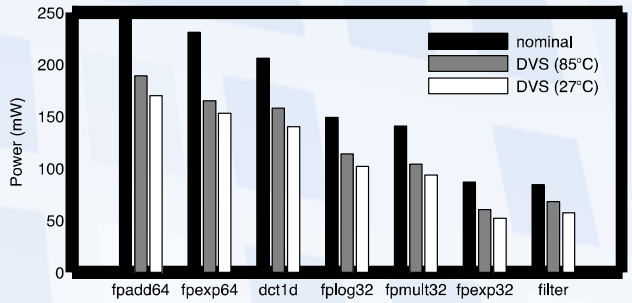


Figure 3. Power comparison with static frequency constrained DVFS

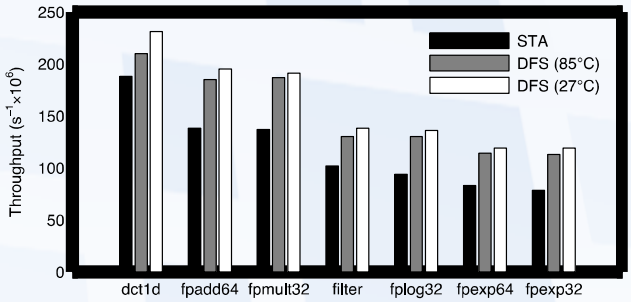


Figure 4. Throughput comparison with static voltage constrained DVFS

Figure 4 illustrates the same for throughput, with static voltage constrained DVFS achieving an average increase in throughput of 31% at 85°C and 39% at room temperature.

Conclusion

Timing margins are required to guarantee reliable operation in current process technologies and these are expected to grow with technology scaling. **PRiME's** DVFS technology can reclaim a significant proportion with little overhead, achieving close to optimal circuit operation and adapting to variation over time. All this can be achieved automatically, for arbitrary circuits using our associated tools.

More information:

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