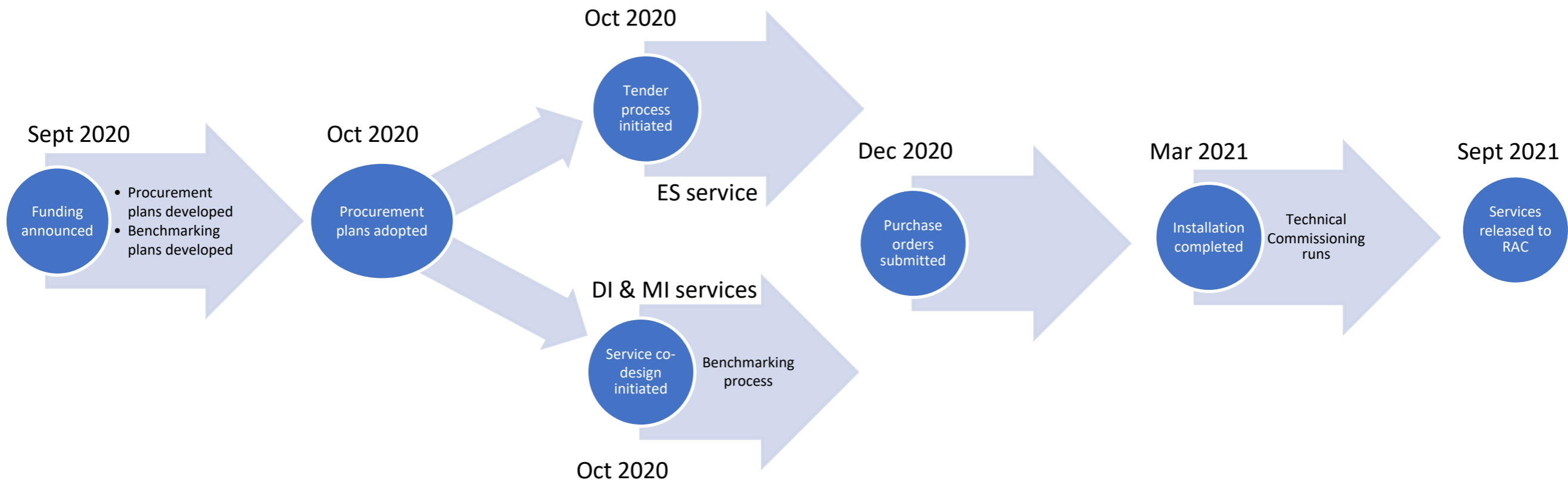# DiRAC Update

Mark Wilkinson, Director

UK LFT Kick-off meeting
24th March 2021

DiRAC-3 Phase 1

UKRI World Class Labs funding

- DiRAC awarded £20m in capital funding to deploy Phase 1 of DiRAC-3

- WCL funds are intended to provide "*critical investment to maintain and upgrade equipment and facilities*"

Sept 2020

Funding announced

- Procurement plans developed
- Benchmarking plans developed

Oct 2020

Procurement plans adopted

Oct 2020

Tender process initiated

ES service

DI & MI services

Service co-design initiated

Benchmarking process

Oct 2020

Dec 2020

Purchase orders submitted

Mar 2021

Installation completed

Technical Commissioning runs

Sept 2021

Services released to RAC

- Technical Commissioning: goal is to optimise systems to deliver DiRAC-3 science programme

- RAC process for October 2021 to March 2021 will be announced shortly

- RAC14 process will follow usual timetable for allocations for April 2021++

DiRAC-3 Phase 1 - hardware

Extreme Scaling "Tursa"

- Supplied by ATOS
- Hosted by Edinburgh
- 112 GPU nodes (4.4 PF):
    - 4x A100-40GB Nvidia GPUs
    - 2x AMD Rome 7302P CPUs
    - 1 TB RAM
- 6 CPU nodes:
    - 2x AMD Rome 7H12 CPUs
    - 256 GB RAM
- Non-blocking HDR200 network
- 4 PB disk storage
- 8 PB tape storage

Data Intensive - Cambridge "CSD3"

- Supplied by Dell
- 260 CPU nodes (~20k cores):
    - 2x 38-core Intel Icelake CPUs
    - 512/256 GB RAM
- 3:1-blocking HDR200 network
- 5 PB disk storage
- 21 GPU nodes (0.8PF):
    - 4x A100-80GB Nvidia GPUs
    - 1TB RAM
    - 2x 64-core AMD Rome CPUs

DiRAC-3 Phase 1 - hardware

**Memory Intensive
"Cosma 8"**

- Supplied by Dell
- Hosted by Durham
- 360 CPU nodes (46k cores):
  - 2x 64-core AMD Rome 7H12 CPUs
  - 1 TB RAM
- Non-blocking HDR200 network
- 4x 1TB fat nodes (AMD 7702 CPUs)
- 6.7 PB disk storage
- 1.2 PB SSD volume
- 20 PB tape storage

**Data Intensive - Leicester
"DIaL"**

- Supplied by HPE
- 200 CPU nodes (26.5k cores):
  - 2x 64-core AMD Rome 7742 CPUs
  - 512 TB RAM
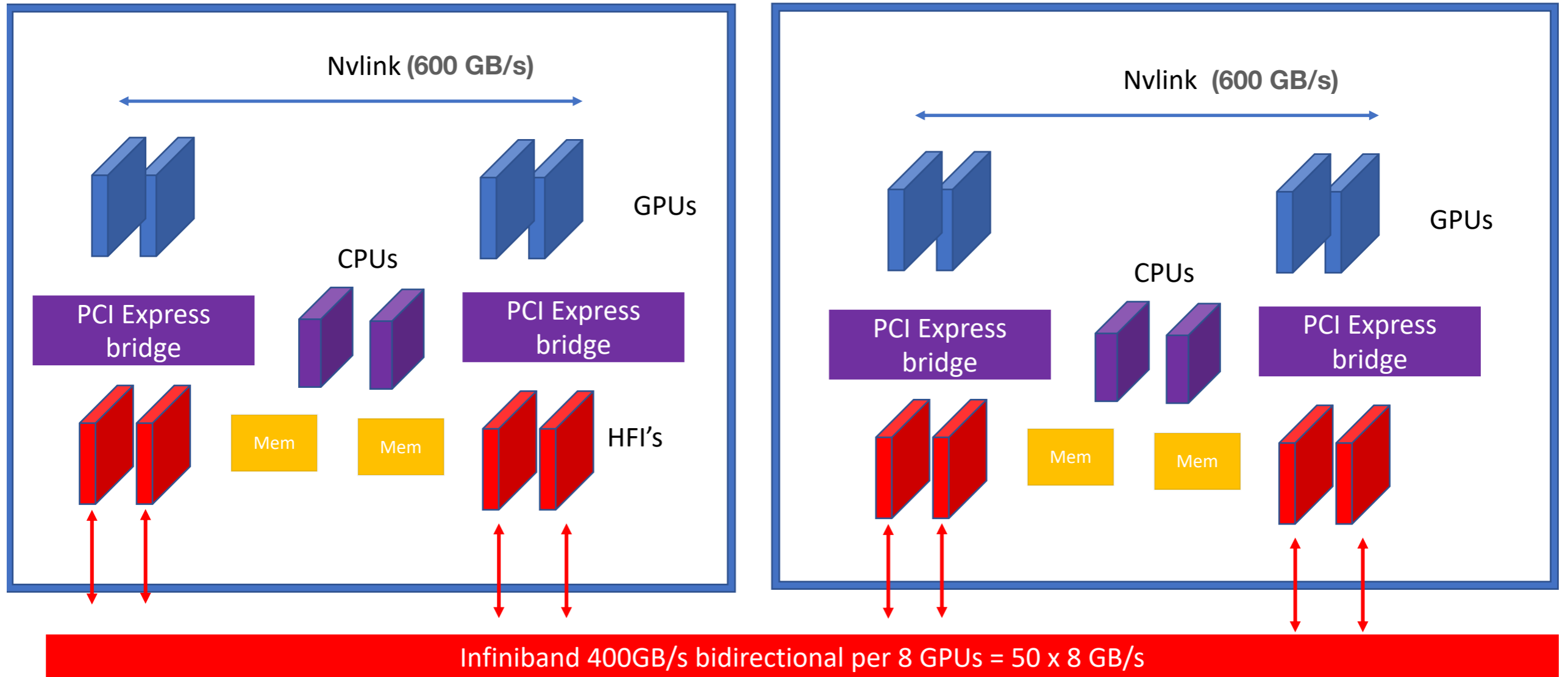- 3:1-blocking HDR200 network
- 4 PB disk storage

DiRAC-3 Phase 1

- Very significant increase in resources:
  - Tursa PF is 2.6x Tesseract PF

- New architecture: Tursa is a possible exascale pre-cursor
  - Think now about how to exploit it….

- Improved power efficiency
 - all new systems use direct liquid cooling

Other aspects of Phase 1 activity:

- 5 RSEs
- Data curation service pilots

Tursa GPU-GPU communication

Nvlink (600 GB/s)

GPUs

CPUs

PCI Express bridge

PCI Express bridge

Mem

Mem

HFI's

Nvlink (600 GB/s)

GPUs

CPUs

PCI Express bridge

PCI Express bridge

Mem

Mem

Infiniband 400GB/s bidirectional per 8 GPUs = 50 x 8 GB/s

Innovation placements

- Recent addition to DiRAC training portfolio

- 6-month placements for PhD students and early-career PDRAs

- DiRAC was initially awarded funding for 8 placements by STFC

  - 12 supported to date
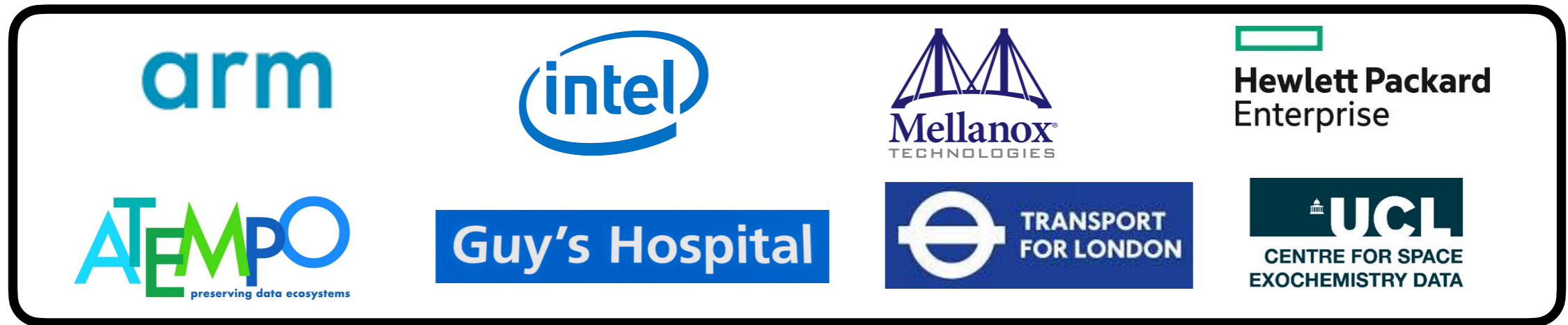
- Funding for at least 3 more placements in 2021 provided by DiRAC-3 partners - more details soon

  - Ideas welcome

- Benefits include:

  - Bi-directional knowledge exchange

  - Enhanced employability

  - Experience of working in industrial environment

  - Skills development

Other training opportunities

Hackathons

- Recent: AMD GPU
- Upcoming: Nvidia GPU; AMD CPU

Upcoming workshops

- OpenACC - delivered by Nvidia
- Cuda - delivered by DiRAC Training Manager Richard Regan

AI-athon

- ML course supported by STFC SciML team

Summary

- DiRAC-3 Phase 1 deployments are imminent

  - Very significant uplift on all services

  - Start thinking now about how to exploit them

- RAC process for Oct-Mar period will be announced soon

- RSE effort available to support code optimisation

- Training opportunities to help prepare for new systems.