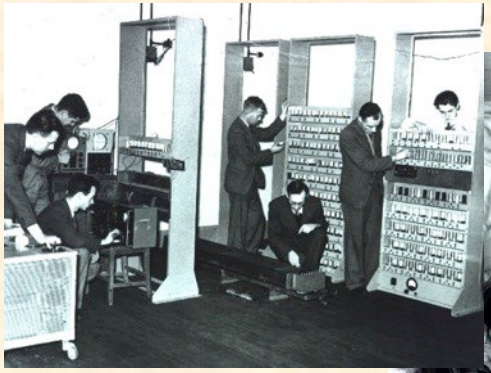
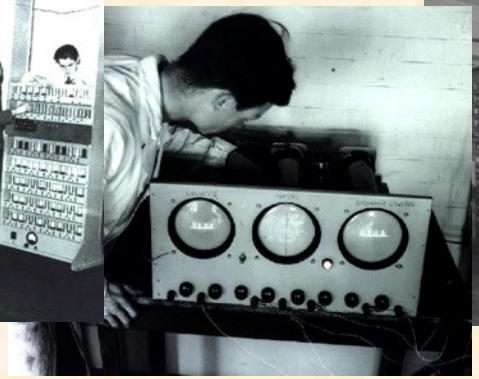
Electronic Delay Storage Automatic Calculator

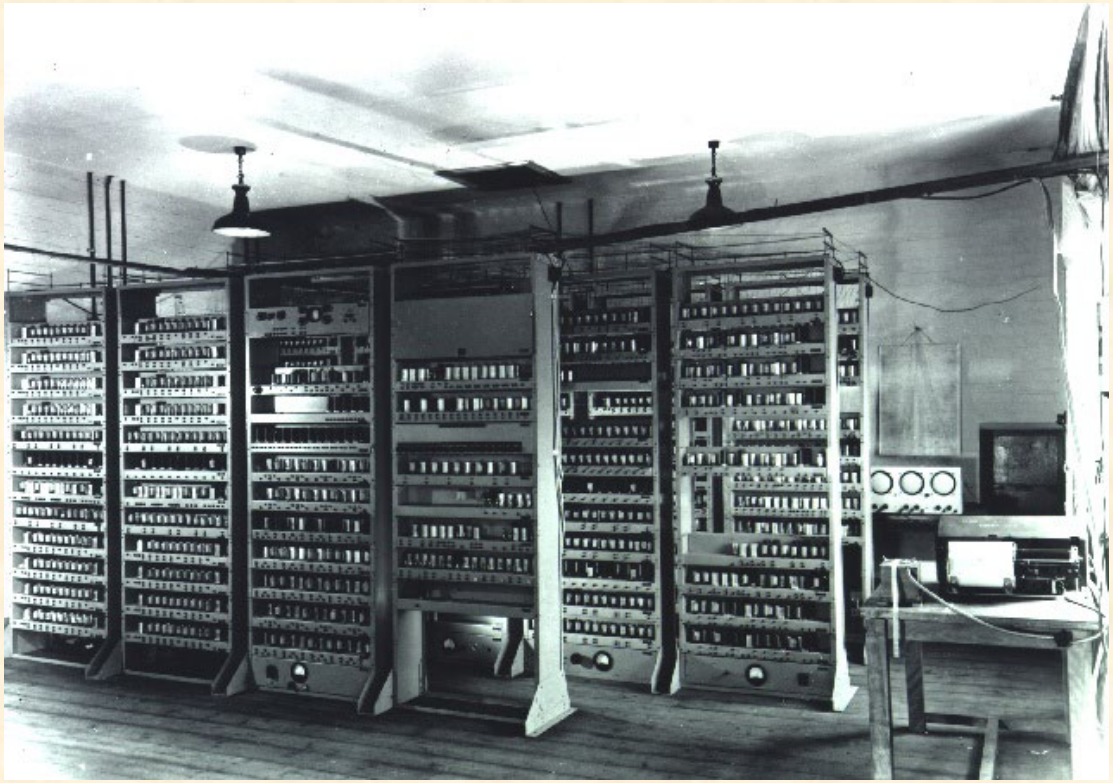



Reconstructing EDSAC

Andrew Herbert

20th March 2024

The Project



Build a working reconstruction of Cambridge University's EDSAC Computer as it was when it provided the world's first computing service in 1950/51.

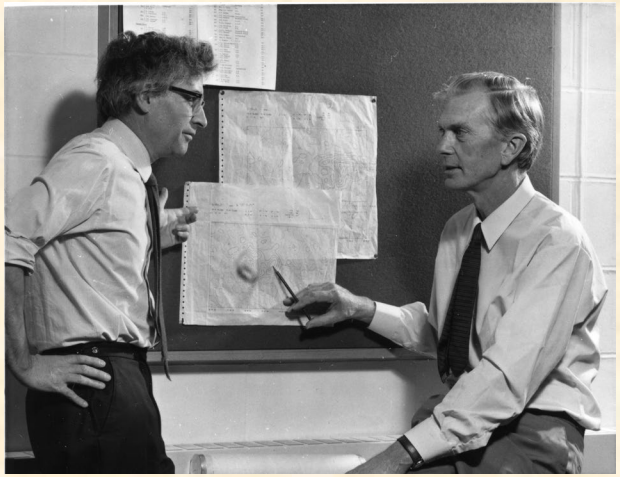
Why Build a Replica of EDSAC?

- To celebrate an early triumph of British computer technology – and the creation of the world's first practical electronic stored program computer.
- To give us a better understanding of our computer heritage and create a new archive of historic material about early computing.
- To revive disappearing expertise and learn about the technical challenges faced by the early computer pioneers.
- A valuable new and living educational resource at The UK National Museum of Computing.

EDSAC Achievements

1. The first *practical* **general purpose, stored program, electronic, digital computer**.
   - provided a *computing service* for the University of Cambridge.
2. The invention of **software**:
   - first machine to read in symbolic programs.
   - Extensive library of "subroutines".
3. Basis for LEO, the world's first business computer.
4. Transformed science:
   - 1500 times faster than the mechanical calculators it replaced.
   - responsible for 3 Nobel Prizes

EDSAC Nobel Prize Winners

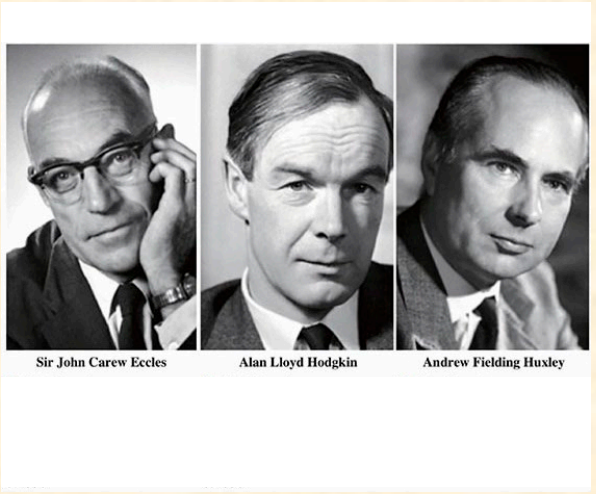


Martin Ryle & Anthony Hewish

Radio Astronomy

Photo: John T Scott,
Physics Today Collection

John Kendrew and Max Perutz
Structure of Globular Proteins
Photo: Medical Research Council



John Eccles,
Alan Hodgkin,
Andrew Huxley

Signalling in the Nervous System

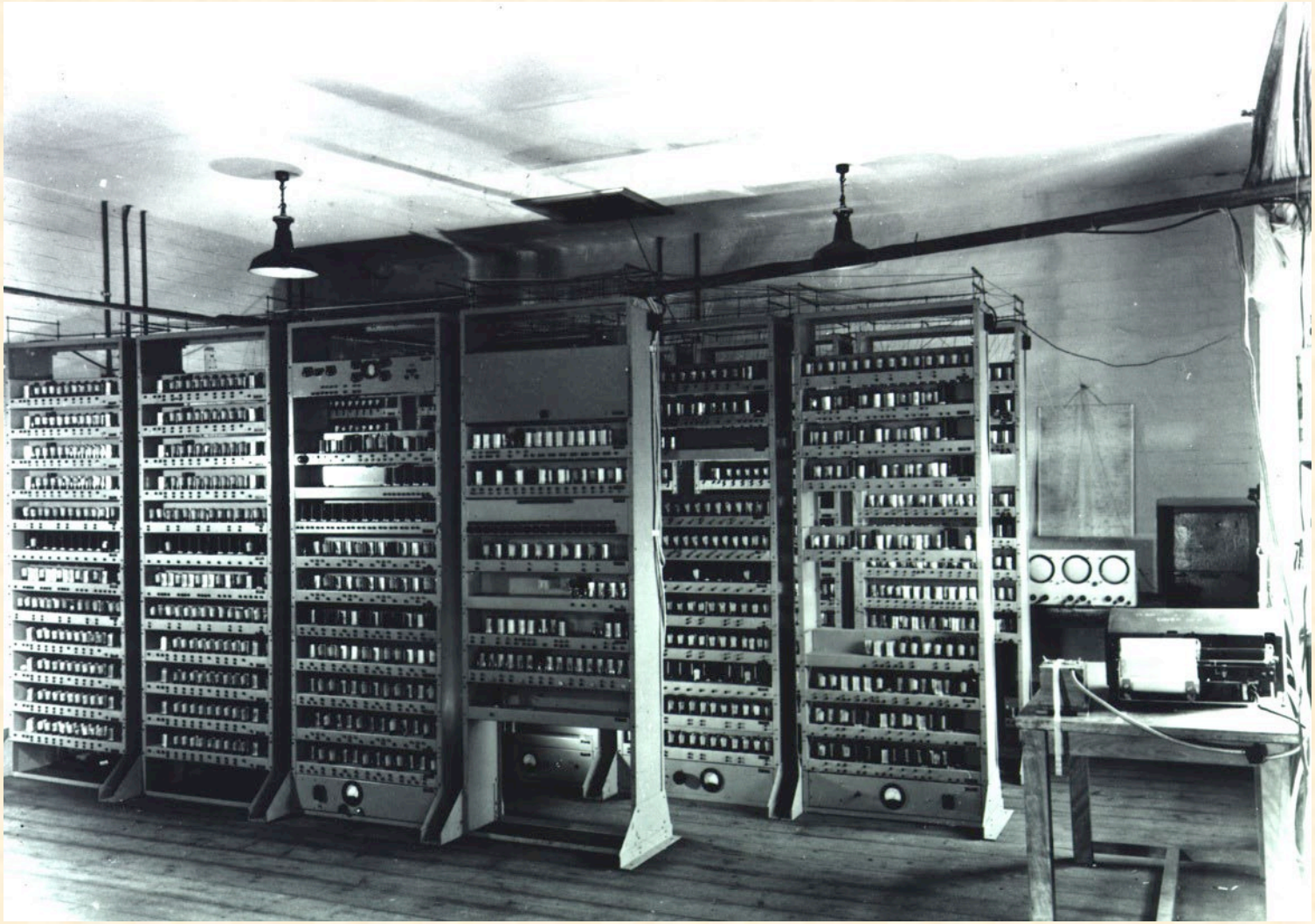
Photo: Nobel Foundation

The EDSAC Story

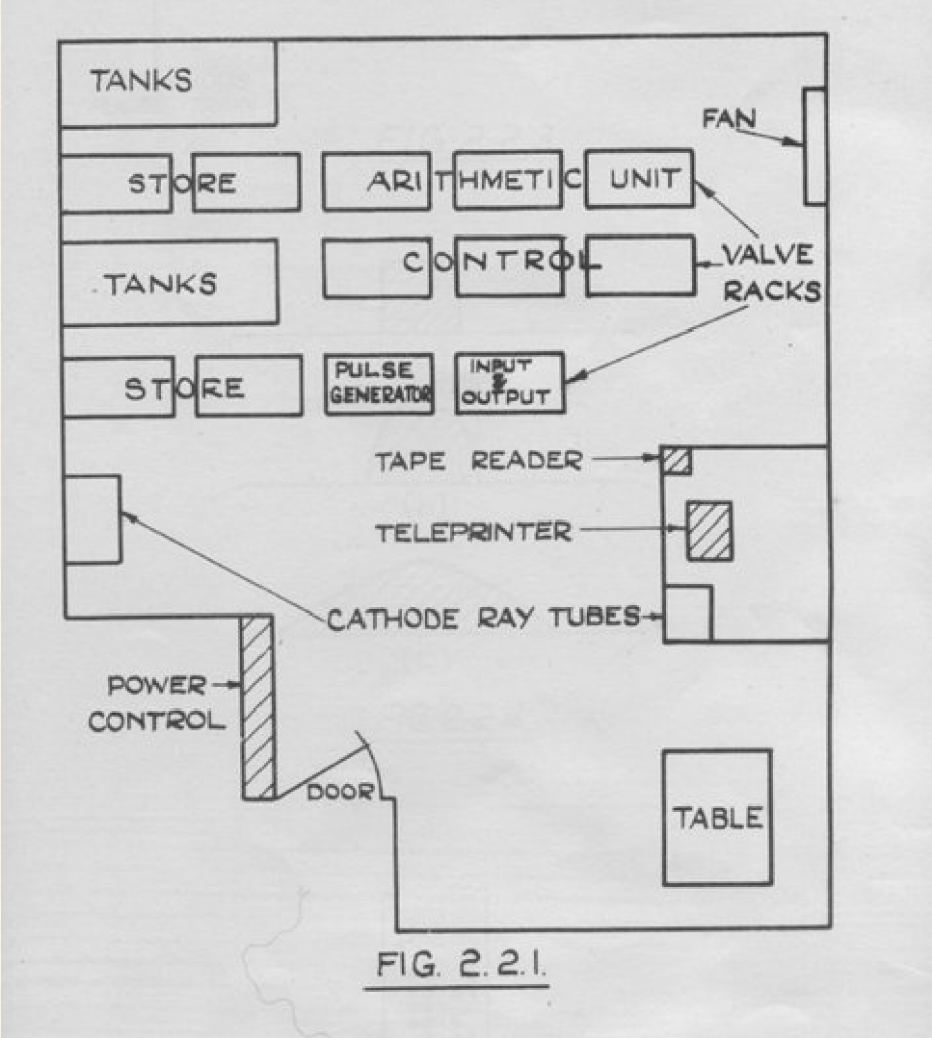
M.V. Wilkes (1913-2010)

- B.A. Mathematics, St John's College, Cambridge
- PhD, Physics, Cavendish Laboratory
- War time radar expert
- Director of Cambridge Mathematical Laboratory
- John Von Neumann: "Draft Report on the EDVAC"
- Princeton Conference 1948

EDSAC (1949)



EDSAC



Dodd & Glennie ARE Report 7/51 1951

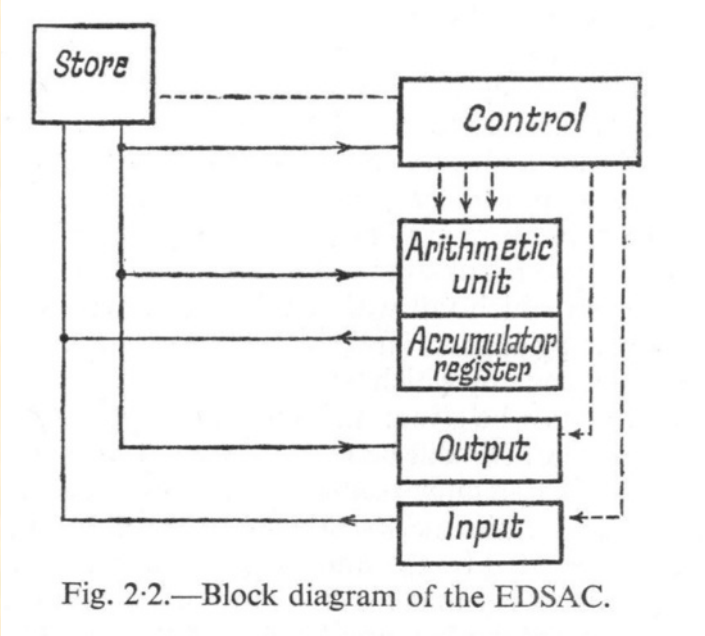


Fig. 2·2.—Block diagram of the EDSAC.

Automatic Digital Computers,
M.V. Wilkes, 1956

EDSAC Architecture

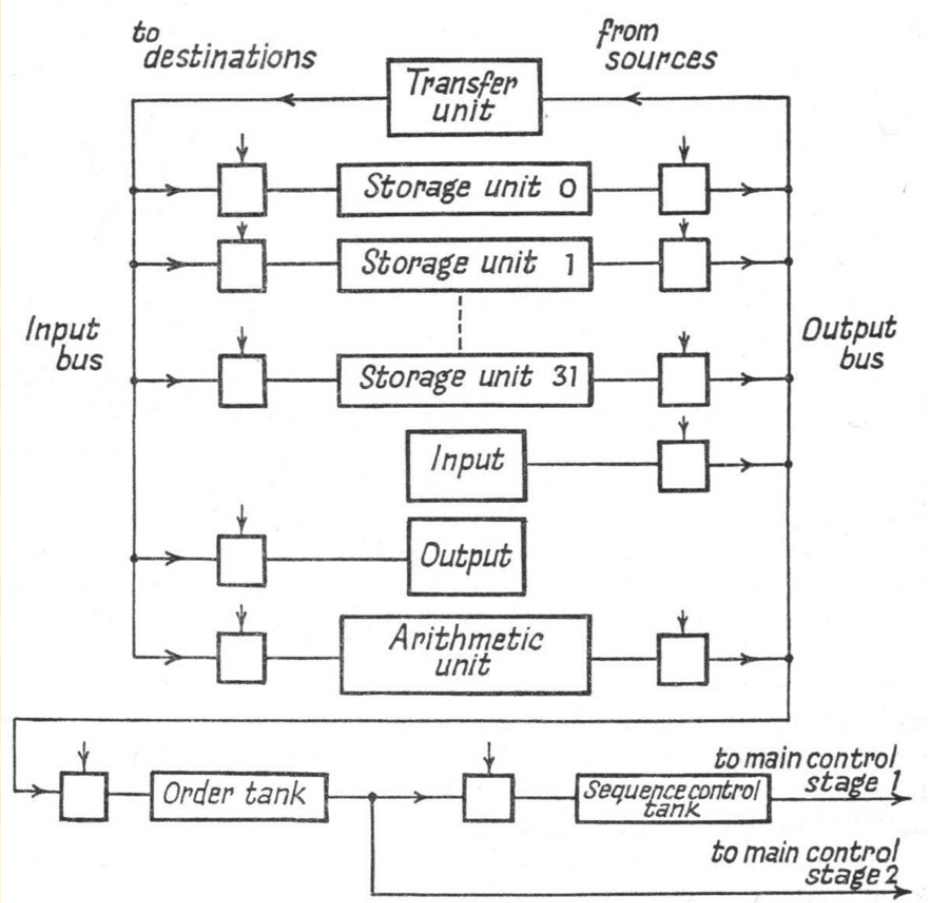


Fig. 2·3.—Numerical interconnexions in the EDSAC.

Automatic Digital Computers, M.V. Wilkes, 1956

Computer Memory in 1949

- Too expensive to build an electronic memory.
  - 5 tubes per bit * 17 * 1024
    = 79,000 tubes.
- Acoustic delay lines.
- Williams (cathode ray) tubes.
- Rotating magnetic drums.
- All were complex, expensive and unreliable.
- All limited speed of the "computer".

EDSAC Acoustic Delay Lines

Maurice Wilkes with a battery of 16 storage tanks, each holding 16 x 36 bit words.

The 5 ft steel tubes contain mercury as the acoustic delay medium.

Designed by T. Gold.

Serial Computing

Most of EDSAC is serial
Process one bit of a word at the time
Reduces number of components needed

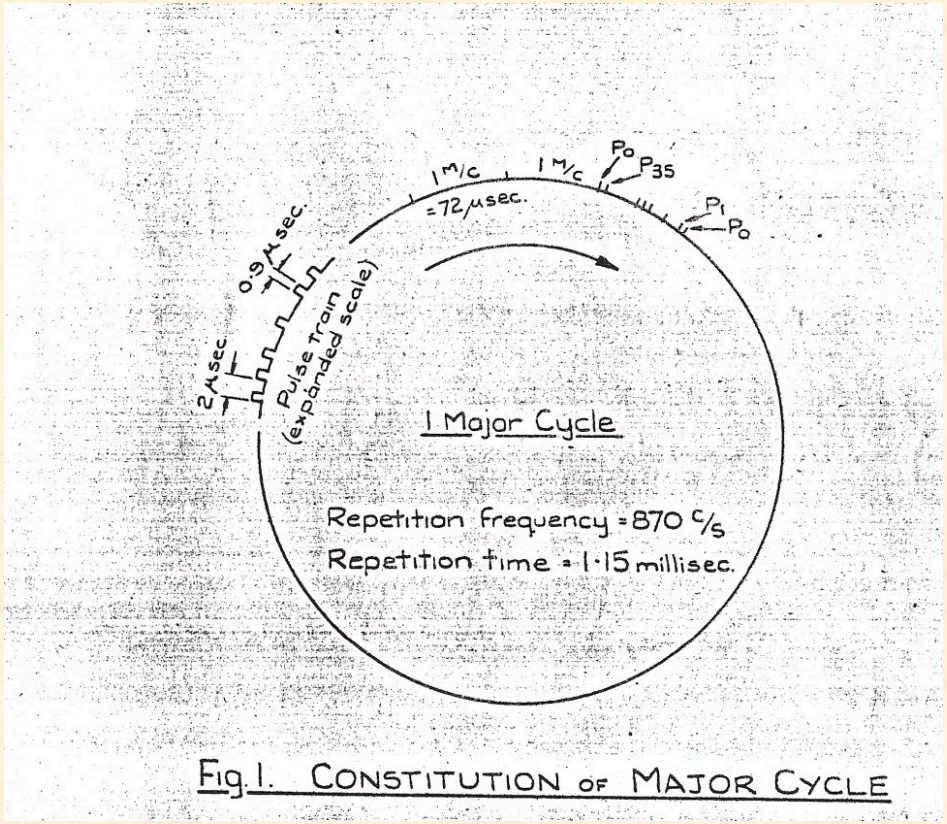


Fig. 1. Constitution of Major Cycle

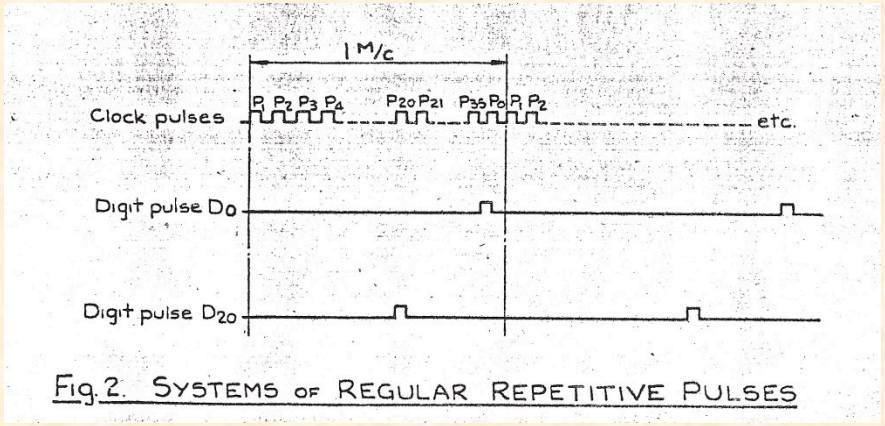


Fig. 2. Systems of Regular Repetitive Pulses

From Edsac Report

Decoding and Coincidence

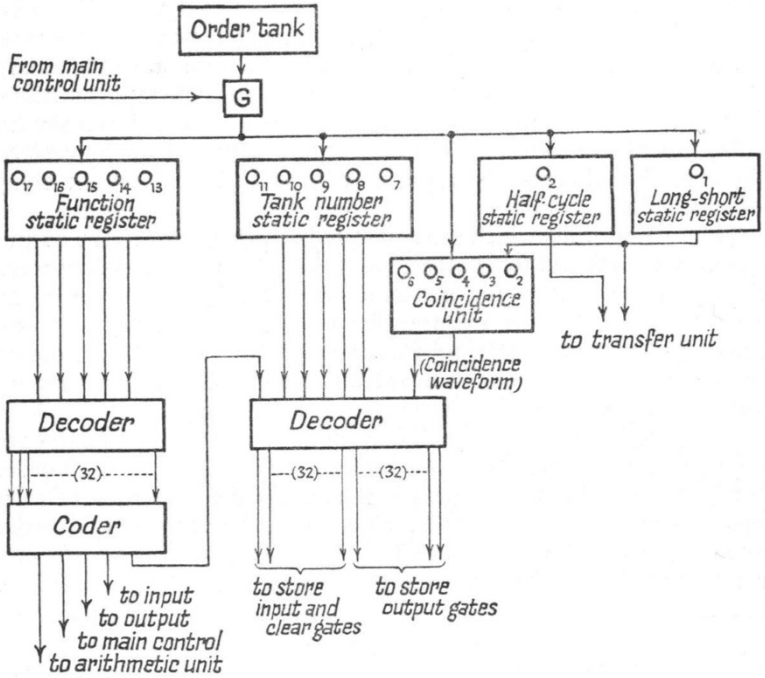
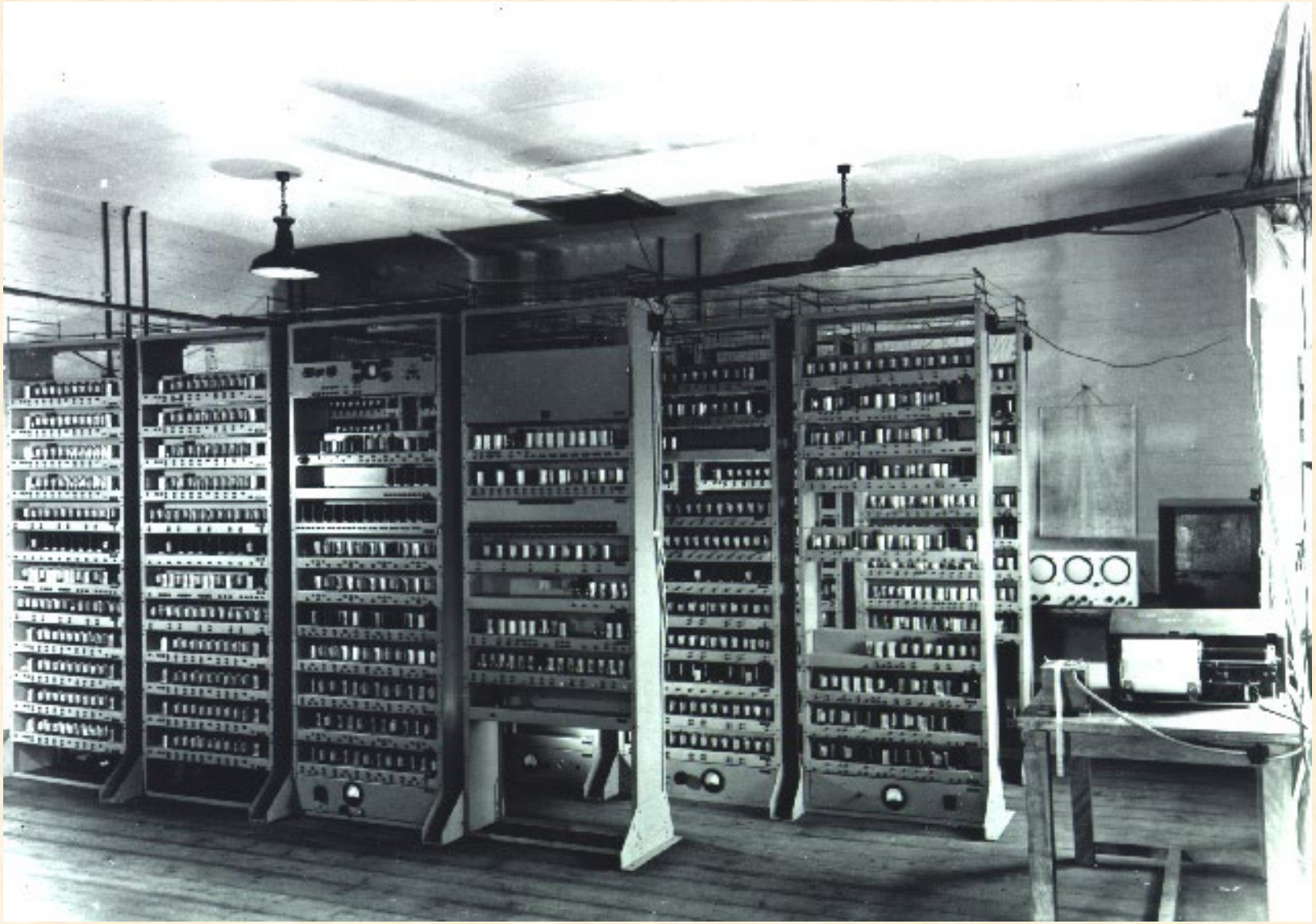


Fig. 2·4.—Block diagram showing how orders are interpreted in Stage II of the control sequence.

Have to go parallel to decode function number and memory address

Automatic Digital Computers, M.V. Wilkes, 1956

Building the Replica



Authenticity

We don't have a complete blueprint,
so we aim to...

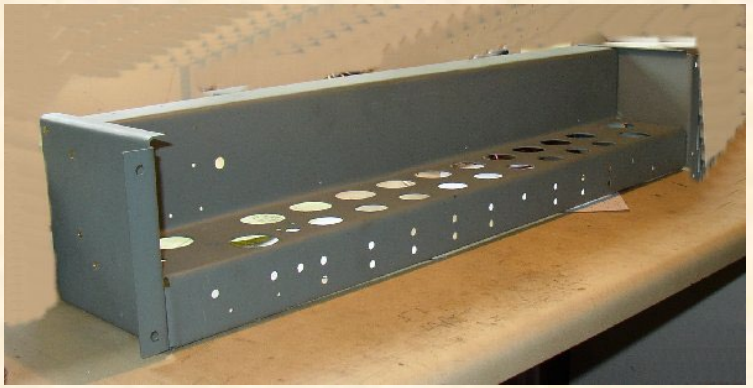
- be consistent with photographs and contemporary records.
- use period components and circuits when available and suitable.
- Use functionally equivalent modern components otherwise.
- adhere to EDSAC "principles" when filling in gaps.

Documents & Knowledge Acquisition

- Original (incomplete) technical description & logical design outline from Cambridge Computer Laboratory archives.
- Original photographs & published papers.
- Recollections of pioneers.
- Recently found cache of ~20 circuit diagrams.
- EDSAC ran for 10 years so need to understand the evolution of the machine (our target: 1950/51).

Mechanical Design

- Scanning and measuring from photos.
- 12 racks, 142 chassis ("panels").
- An original chassis exists to measure.
- Drawn up using CAD.
- At the outset we didn't know how many different types of chassis there were, or where they were placed in the racks.



Rack and Chassis Manufacturing

Teversham Engineering, Cambridge

Logic Design & Simulation

- Need to know how EDSAC works in detail
- Incomplete & inconsistent diagrams
- Evidence of much re-design during commissioning
- Need to extrapolate undocumented areas of logic
- Simulation essential to give confidence before committing to building anything

Typical Logical Diagram

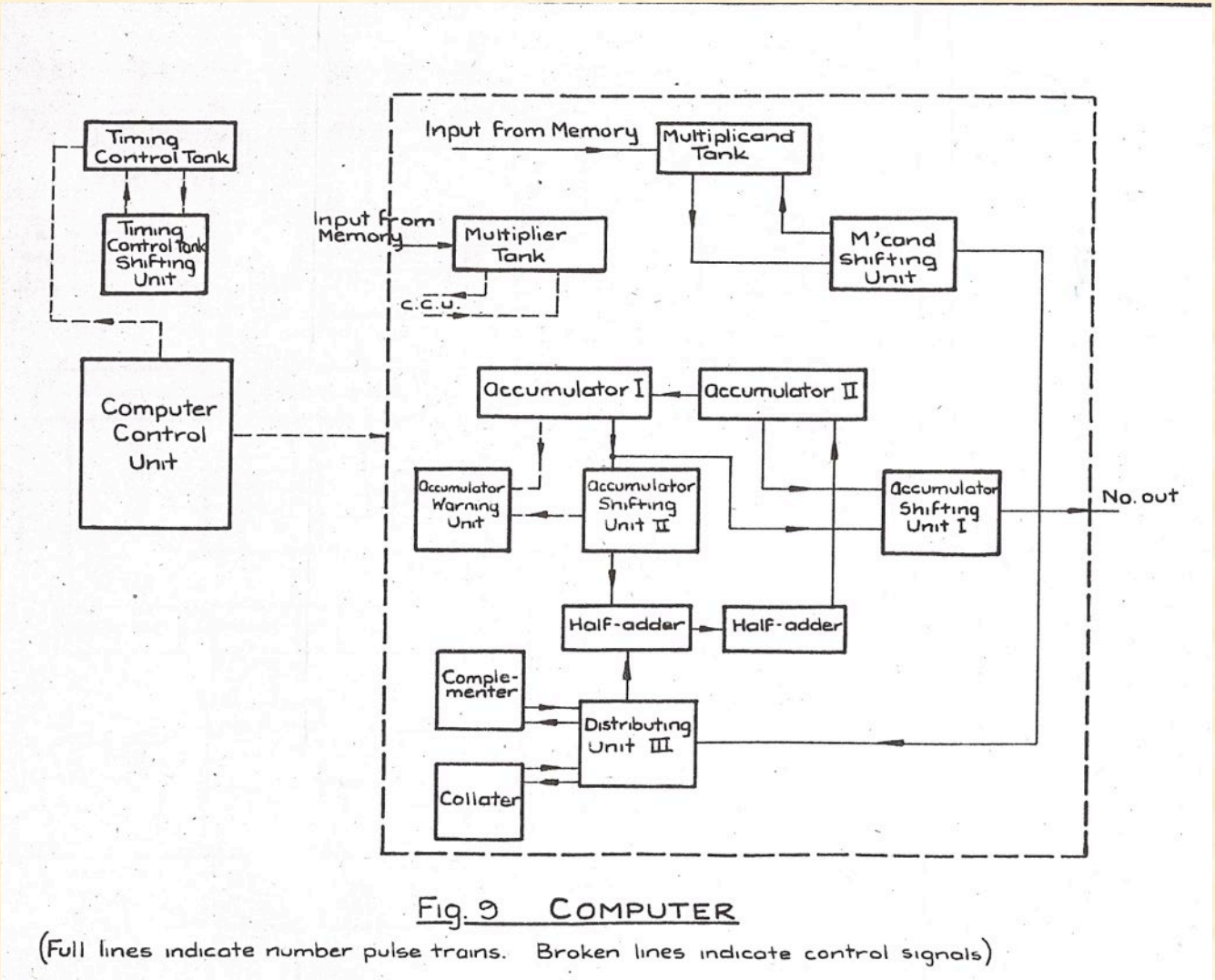


Fig. 9 COMPUTER

(Full lines indicate number pulse trains. Broken lines indicate control signals)

From EDSAC Report

Typical Timing Diagram

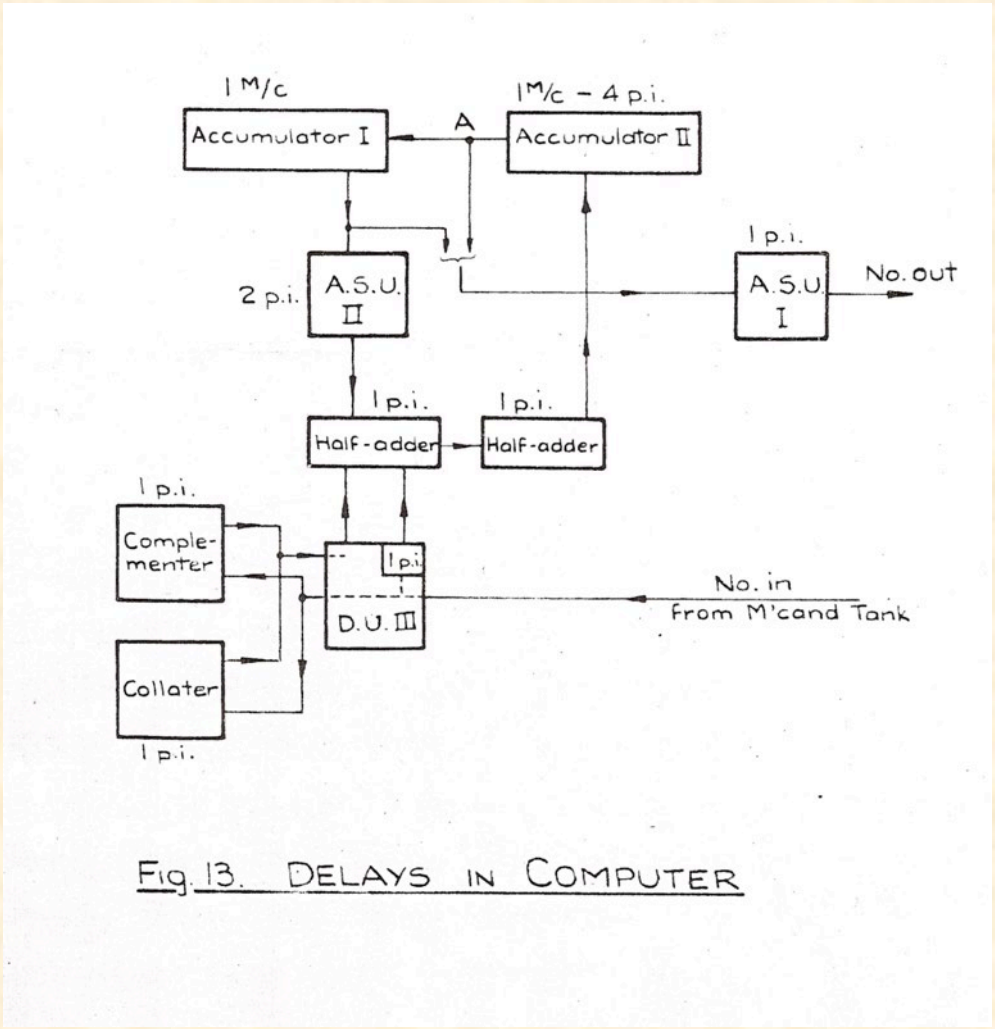
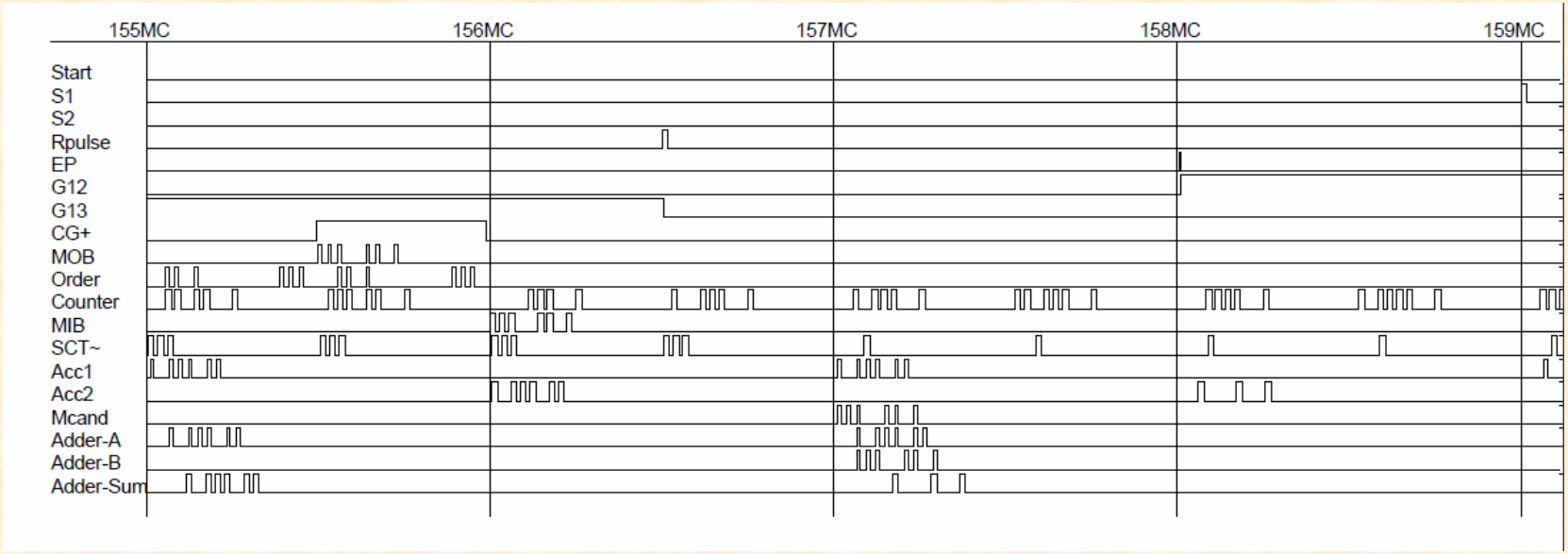


Fig. 13. DELAYS IN COMPUTER

From EDSAC Report

Logic Simulation

- Bill Purvis wrote a simulator for whole logic - can run a program, very slowly.
- Now translated to Verilog and running on an FPGA.



Electronic design

- EDSAC was built by radio and radar engineers: AC-coupled circuits and analogue waveforms.
- Digital logic is expensive - AND-gate uses 3 pentodes and 3 diodes => space saving shortcuts => imperfect circuits.
- Common circuit elements aid identification: flip-flop, inverter, short delay, pulse amplifier.
- Experiments show stage delay is very short and system requires careful tuning to ensure signals arrive "on time".

Typical Circuit Diagram

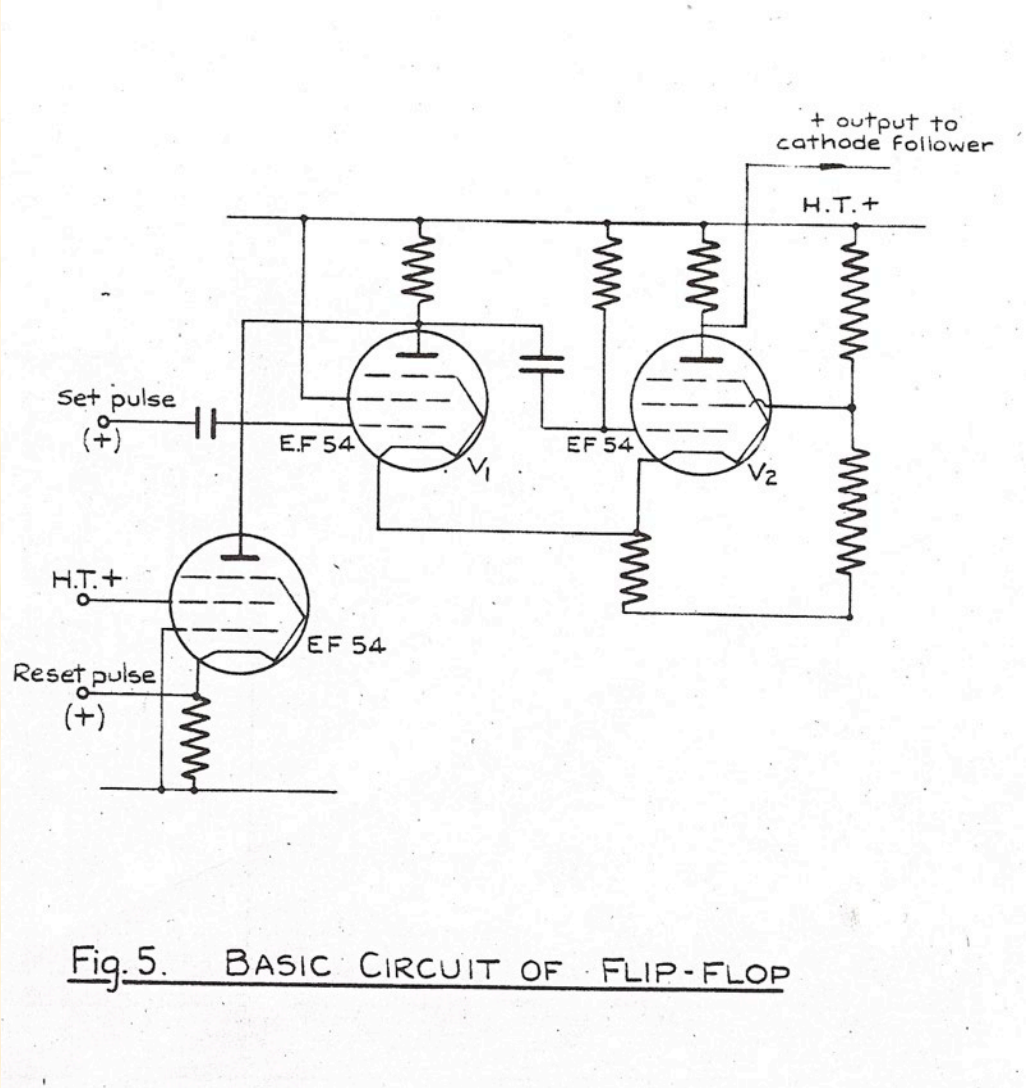
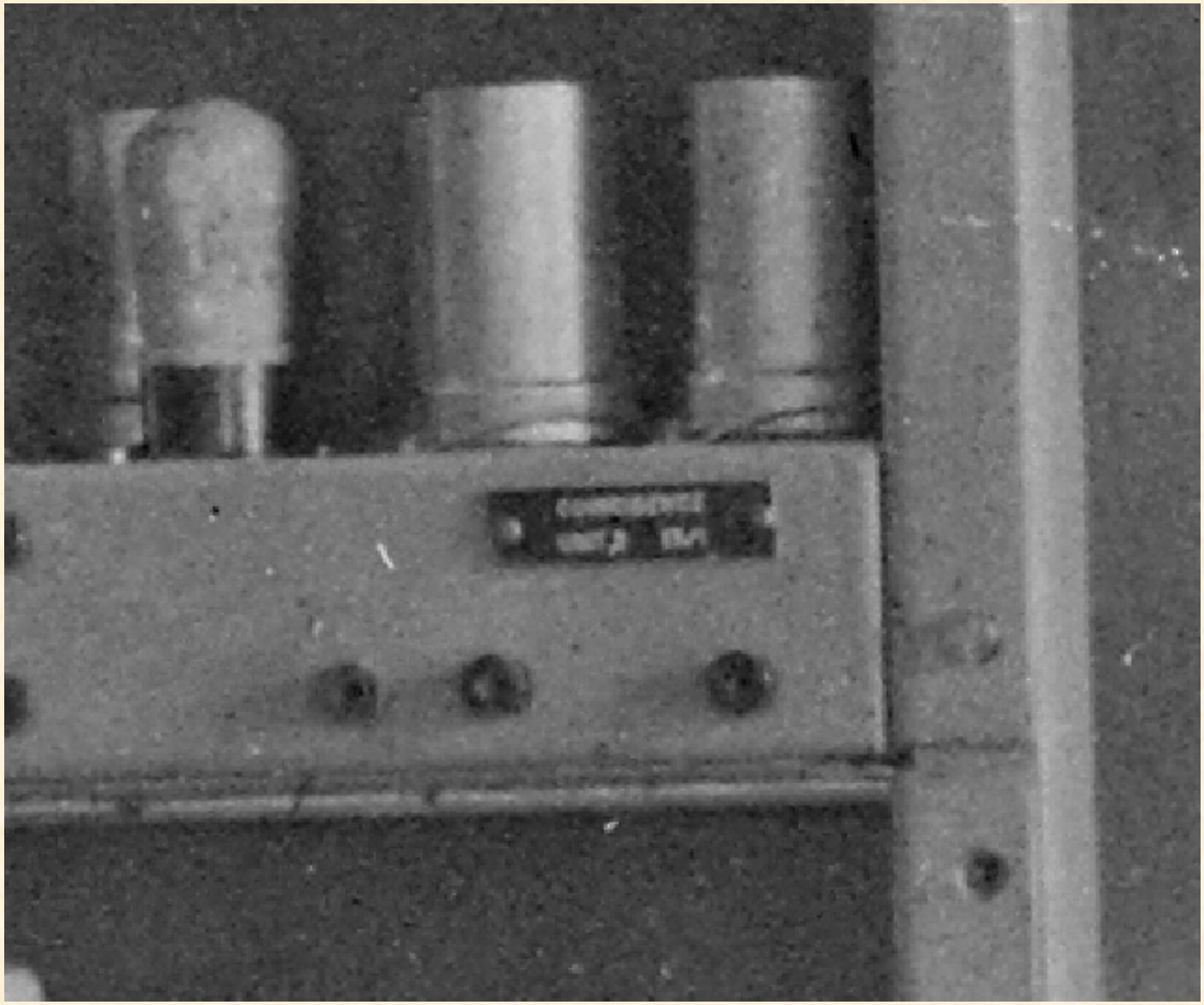


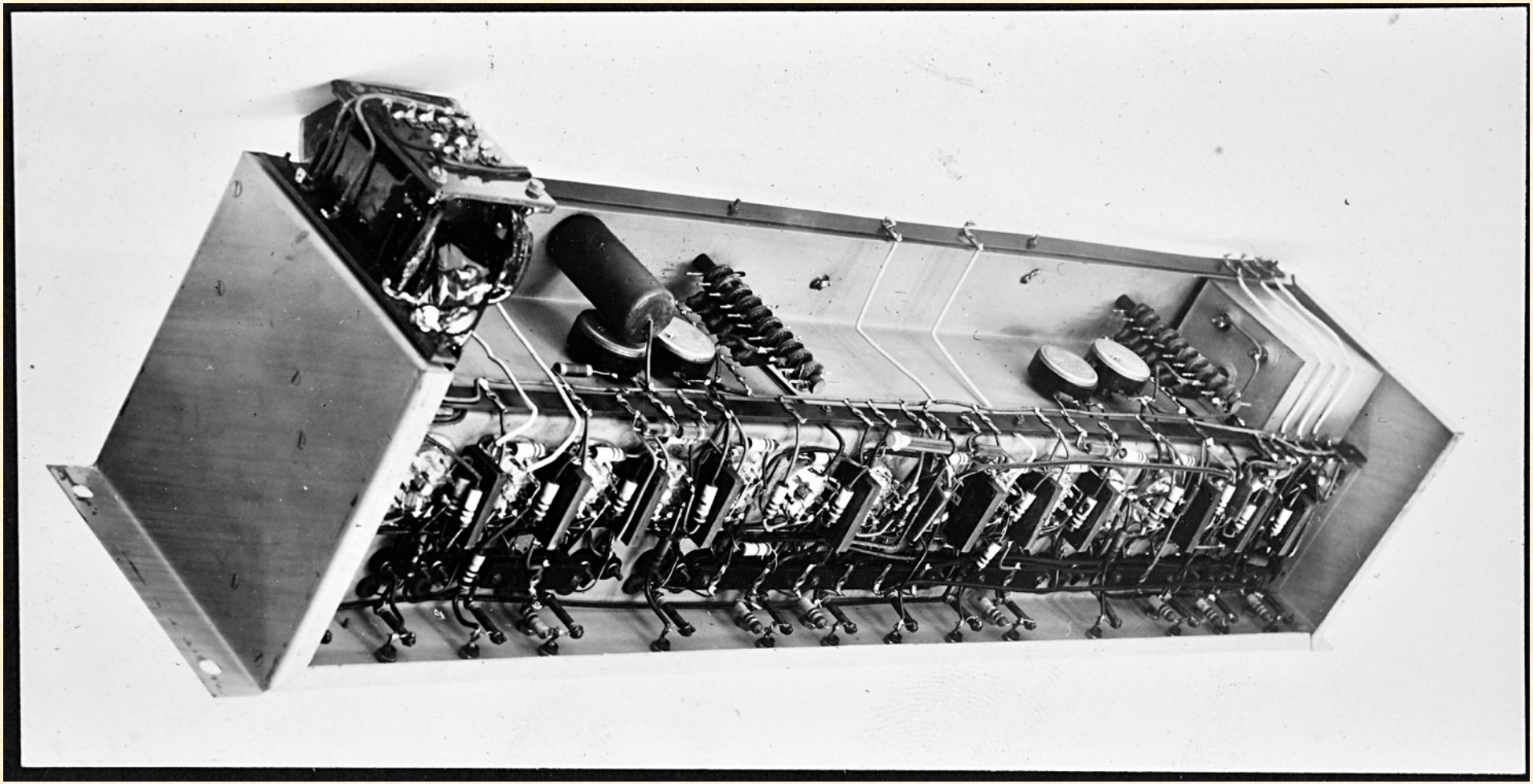
Fig. 5. BASIC CIRCUIT OF FLIP-FLOP

From EDSAC Report

Mapping Logic to Chassis

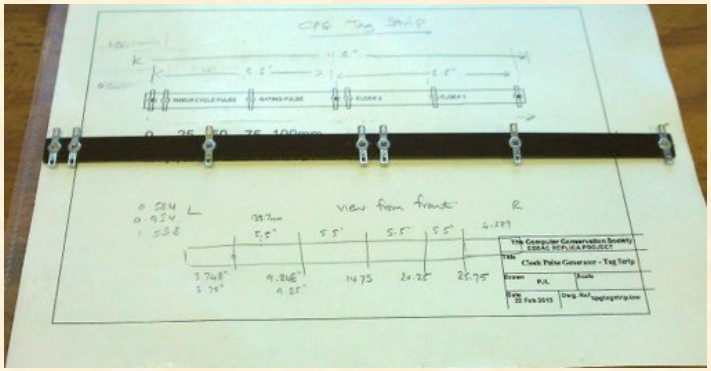


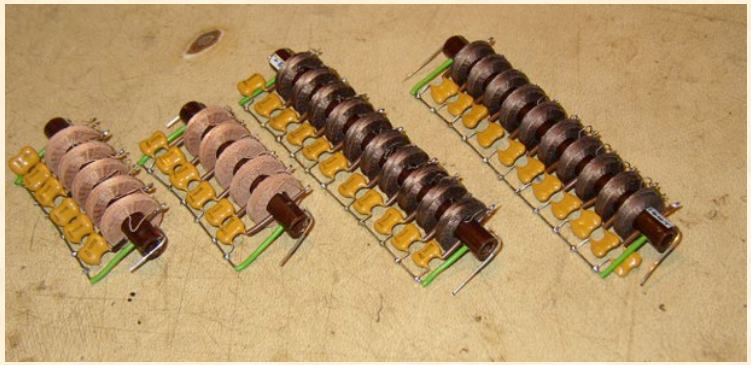
1949 Chassis



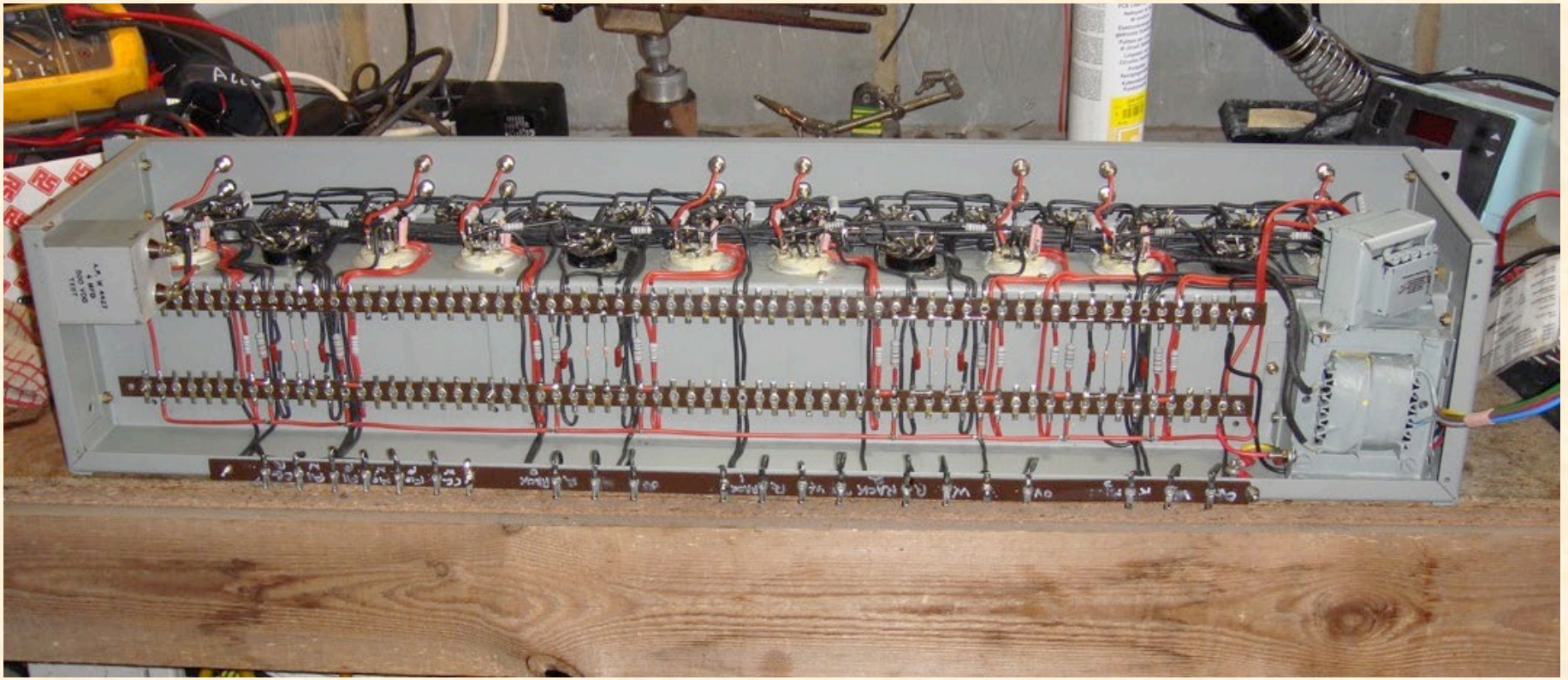
Acquisition of Parts

- Many, but not all, thermionic valves are available commercially as "new old stock".
- B9G valve holders are problematic.
- Authentic 'period' resistors and capacitors are too unreliable to use.
- Hand made tag strips and coils.





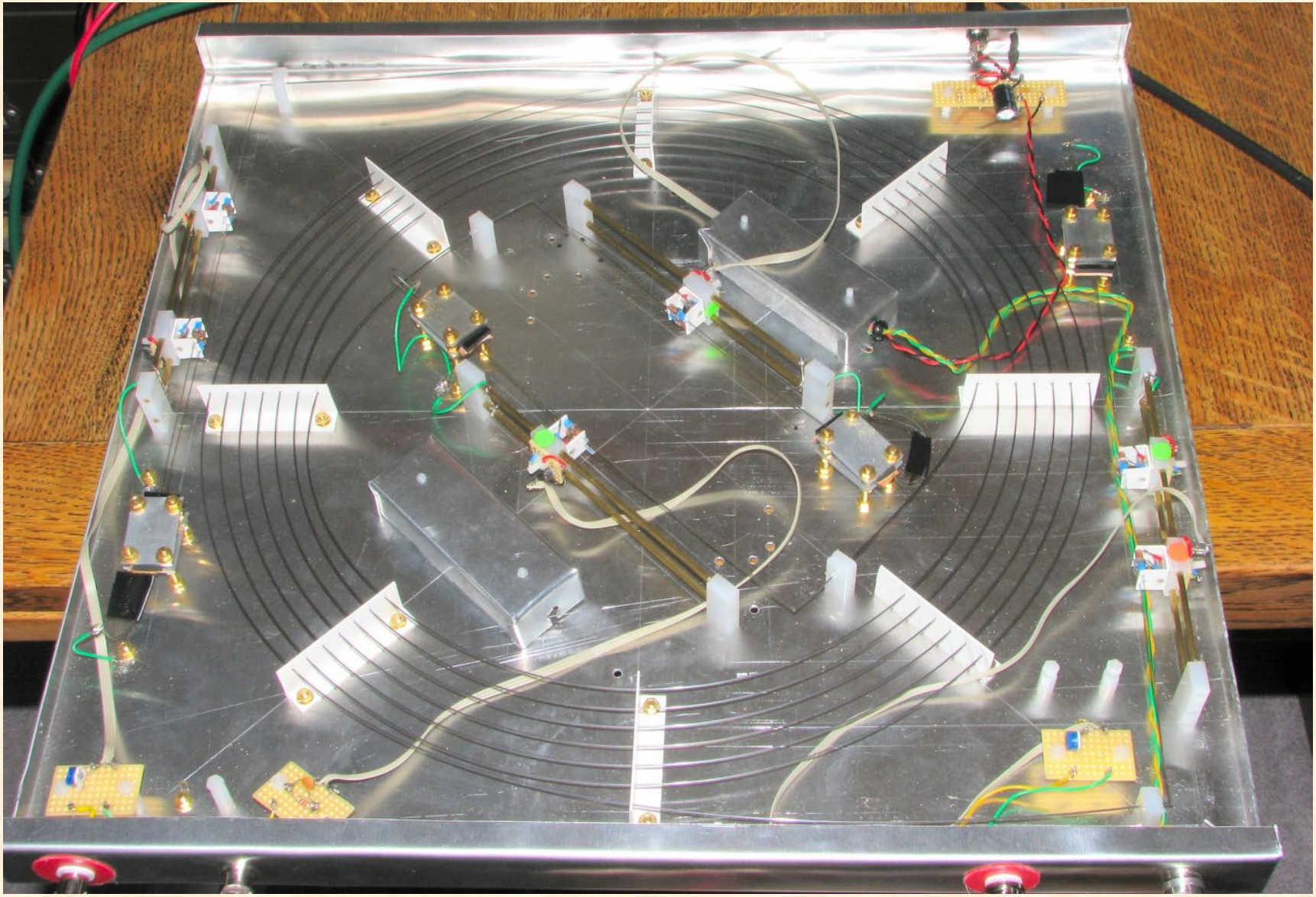
Replica Chassis



Replica Memory Tanks

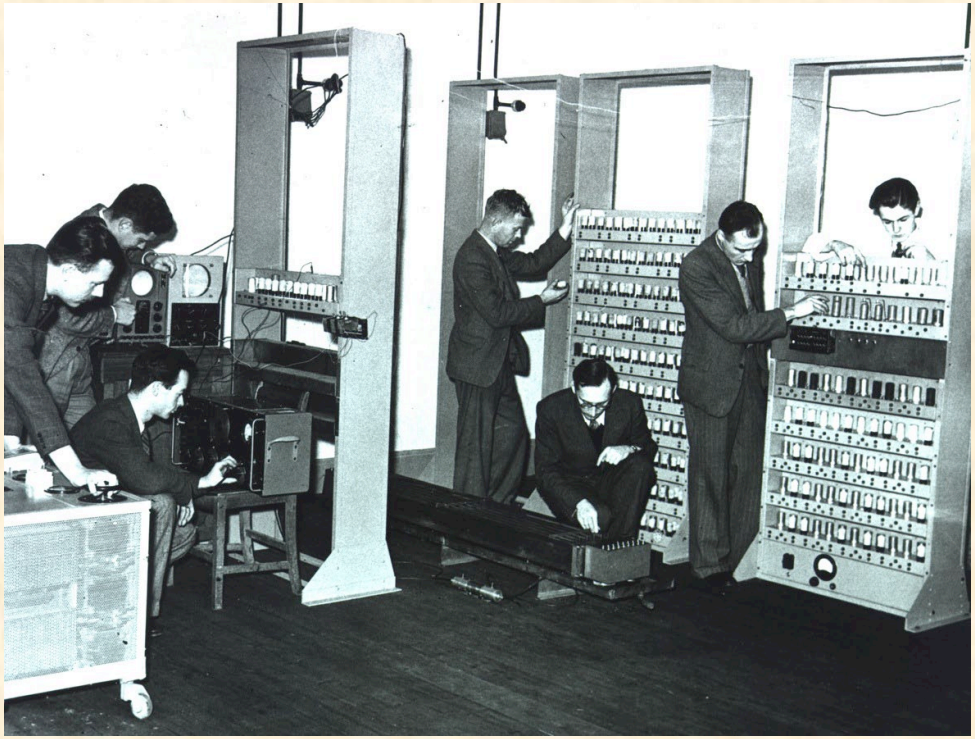
- Risky and costly to use mercury, except perhaps in one example tank.
- Temperature stability is a major issue.
- Precision engineering required: tubes and end plates – aligned to within 0.001" end-to-end.
- Using magnetostrictive nickel delay lines as a reasonable alternative.
- Use semiconductor shift registers to get off the ground quickly.

Short Nickel Delay Line



The Original EDSAC Team

M.V. Wilkes and W. Renwick



The Reconstruction Team

Timeline

- 2010: feasibility study, charity set up, budget (£250,000), founder donors
- 2012: Further fund raising, volunteer recruitment, forensic engineering research
- 2013: Design, prototyping starts
- 2014: Construction starts
- 2015: Commissioning starts
- 2015/Q4: Final round fund raising
- 2018/Q3: First running test program
- 2023/Q4: completed?

Status (March 2024)

- 140 chassis built and tested of 142 total.
- Clock and Digit Pulse system working.
- Memory recirculation, addressing and coincidence working.
- Main control working.
- Transfer unit working.
- Delay line register stores working.
- Main store delay lines in commissioning.
- Systematic testing of arithmetic functions underway
- I/O and Initial Orders under construction

EDSAC Monitoring Architecture

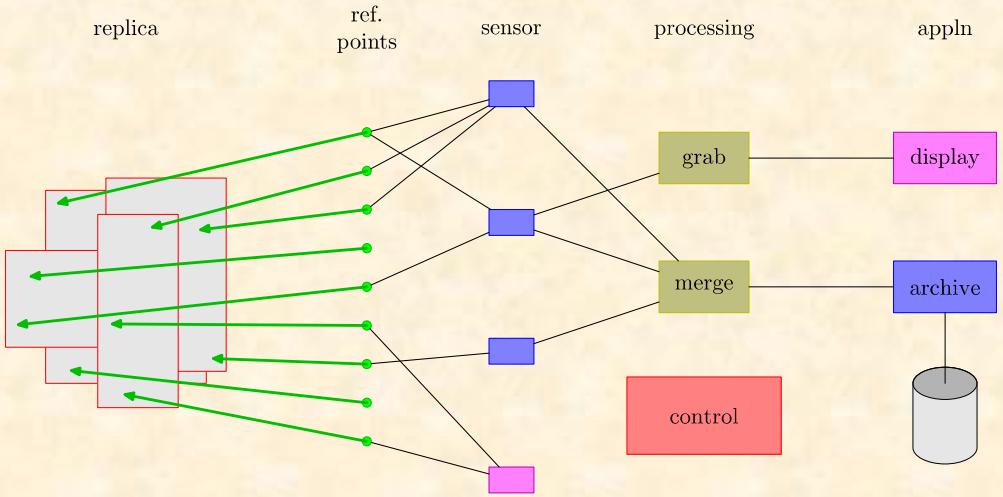


Figure 1: The main data flows in the EDSAC Monitoring System.

- Sensors: EDLA microcontroller-based 16 channel probe, with common timestamp
- Server: Raspberry Pi – commands sensors to capture signals
- Sensor sends captured data over Wifi to server
- Server uses timestamps to merge data
- Archive held as SIGROK files
- Applications to scan files to check for errors, signal degradation, etc, etc

To Find Out More

- Visit www.edsac.org web site
- Download EDSAC simulator from http://www.dcs.warwick.ac.uk/~edsac/