Communication the next resource war

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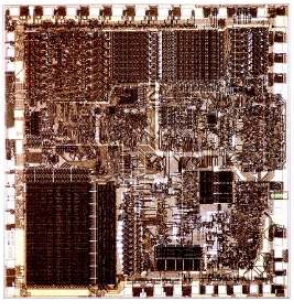
Wires stopped scaling 40 years ago



Intel 8086 (1978)
29,000 transistors
3μm process

Intel Pentium-4 (2000)
42,000,000 transistors
0.18μm process

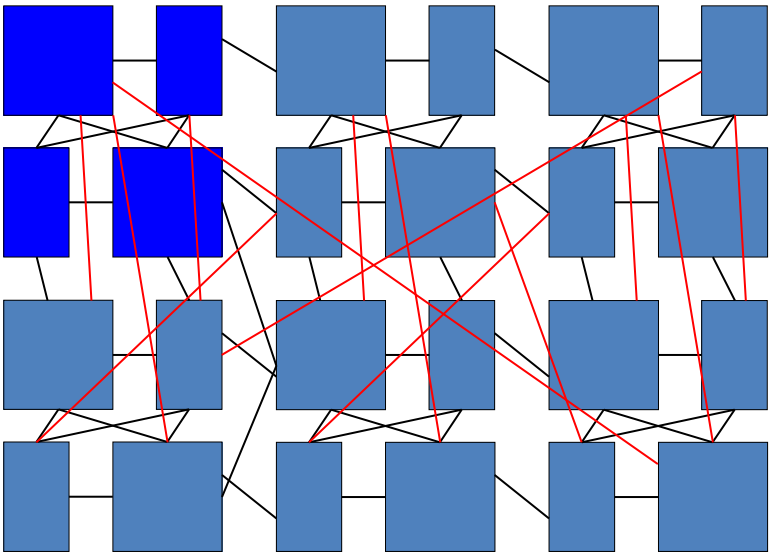
Observation

technology scaling favours transistors over wires

Power of Computation vs. Communication

technology node	130nm CMOS (2006)	45nm CMOS (2008)
transfer 32b across-chip	20 computations	57 computations
transfer 32b off-chip	260 computations	1300 computations

Designs need more wiring (Rent's rule)



Observation: new design criteria

~~computational~~ complexity

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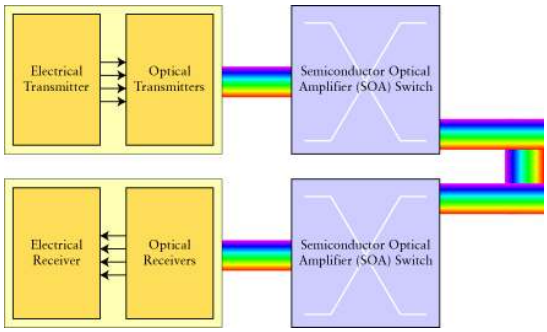
communication complexity

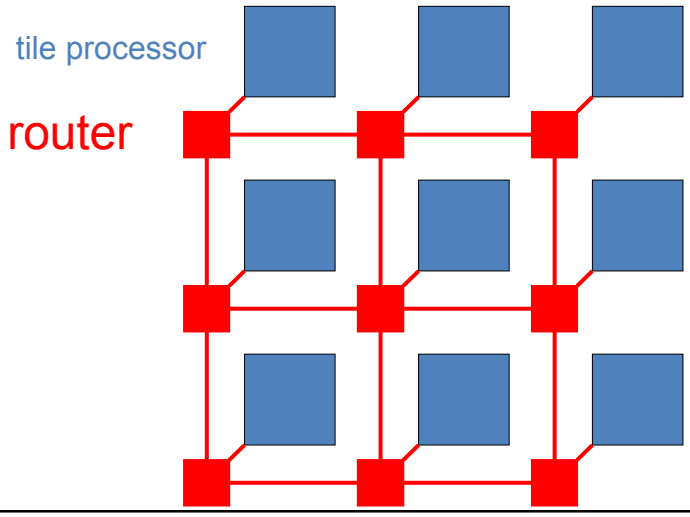
Research: chip-to-chip comms

- multiple-wavelength optical networks funded by Intel
- electronics optimises photonics



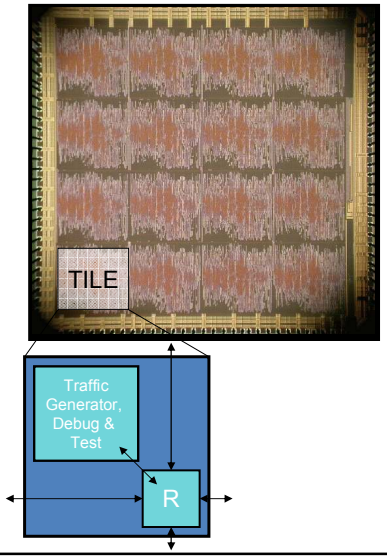
Research: communication on-chip

- Virtualise long wires: Networks-on-Chip



Example Network-on-Chip

- low-latency speculative router prototype chip
- substantially beat Stanford designs



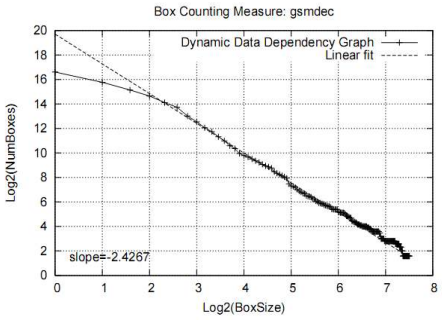
Research: dynamic routing on FPGAs

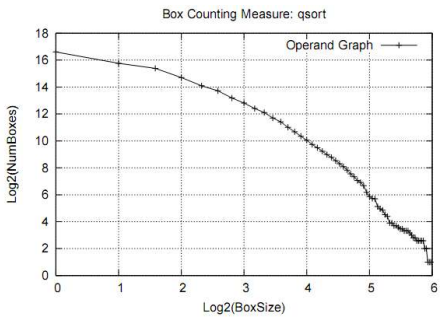
- 3 levels of interconnect:
  1. static routing (as we have already)
  2. simple dynamic (TDM) routing
  3. network-on-chip

Communication complexity in software

Recent result:

- we have identified self-similar (fractal) communication behaviour in many





Research question

How can we optimise communication from transistors & wires to software?

Performance

Sustainability

Power

Research Directions

- £750k EPSRC funding…
- Build high performance reconfigurable simulator using FPGAs
  - 1000 processors
  - communication architectures
  - VLSI equivalent power measures
  - near real-time performance
- Research into languages/compilers/mapping

Conclusions

- The electronics design revolution: think communication complexity not computation complexity
- Electronic technology issues demand more cunning design
- Chip design increasingly about parallel, fault-tolerant, communication-centric algorithms
  - Research at the Computer Laboratory Computer Architecture Group

µGC3 – Moore for Less

- Next meeting in Cambridge 30th Sept
- Theme: how to deliver Moore's law through better design
  - circuits & synthesis for nano CMOS
  - reliable technology on unreliable platforms
  - computer architecture
  - algorithm mapping
    - to hardware & software
    - exploiting parallelism