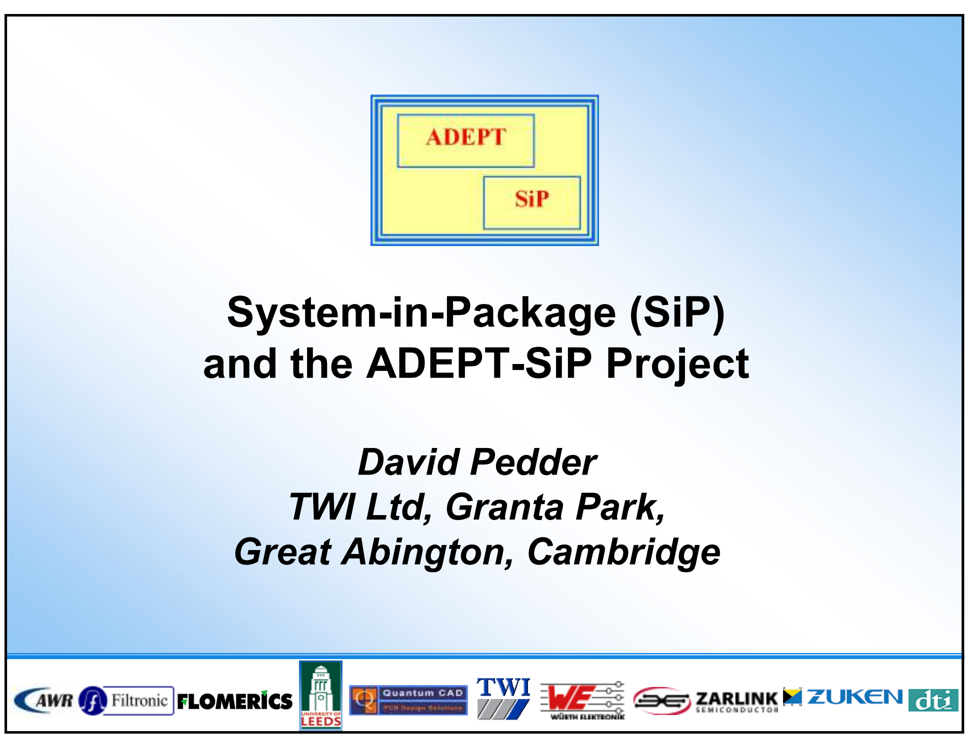
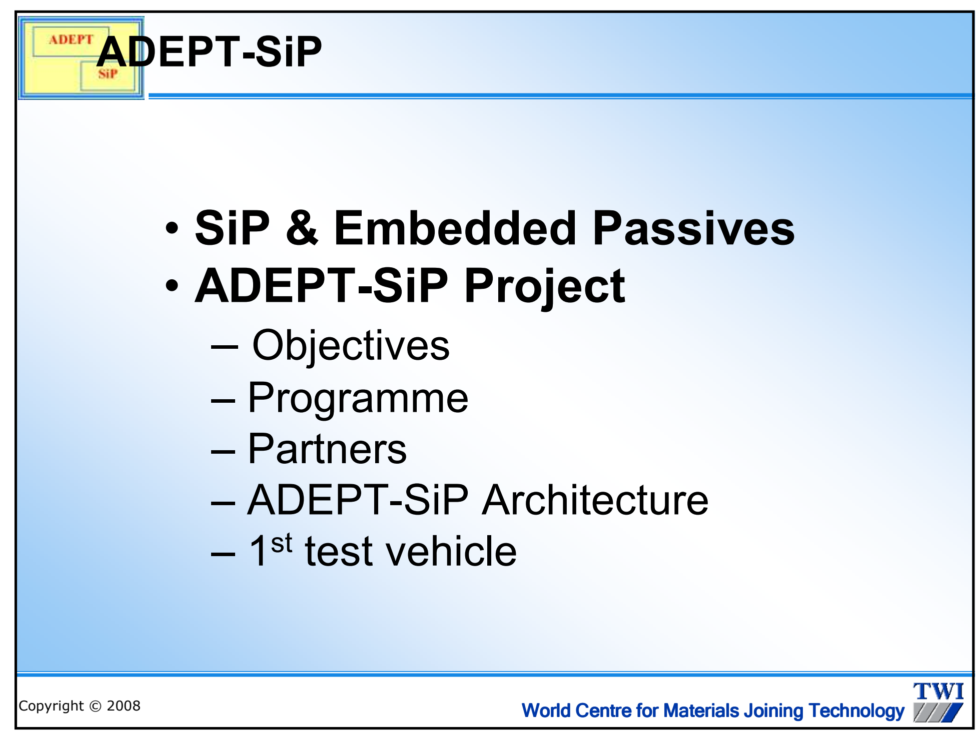

ADEPT
SiP
System-in-Package (SiP)
and the ADEPT-SiP Project
David Pedder
TWI Ltd, Granta Park,
Great Abington, Cambridge
AWR
Filtronic
FLOMERICS
UNIVERSITY OF LEEDS
Quantum CAD
TWI
ZARLINK
SEMICONDUCTOR
ZUKEN
dti


ADEPT
SiP
ADEPT-SiP
• SiP & Embedded Passives
• ADEPT-SiP Project
– Objectives
– Programme
– Partners
– ADEPT-SiP Architecture
– 1st test vehicle
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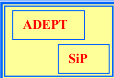
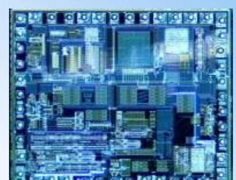
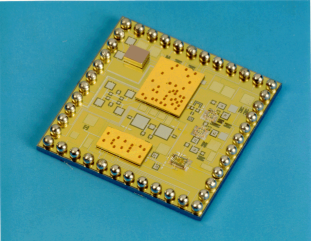


System-in-Package

- System-on-Chip (SOC)
  - Low cost in volume
  - High NRE costs
  - Performance compromises
- System-in-Package (SiP)
  - Multiple active & passive die
  - Standard package outline
  - Stacked Die, modules, MCMs, 3D
  - Flexibility
  - Faster time-to-market
  - Lower NRE
  - Higher performance





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Discrete passive components

On a typical PCB, discrete passives comprise:

- 91% of components
- 29% of solder joints
- 41% of board area
- Last year, ~ 1 trillion passives surface-mounted
- ~ 0.5 cents purchase + 1.3 cents "conversion"
- Passives numbers growing

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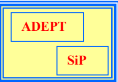

Embedded Passives Benefits

- Improved performance
- Reduced size & weight (2 to 10 fold)
- Higher functional density
- Reduced mounted component count
- Reduced costs per function
- Reduced wiring demand
- Greater SMT throughput
- Improved reliability & EMC emissions
- Continuous component values

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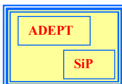
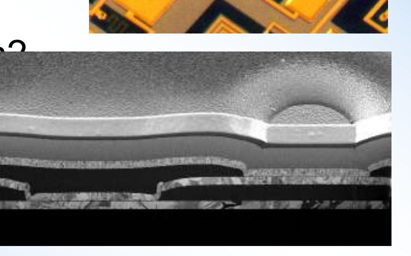


Thin-film passives

- **Substrates**
  - Silicon or glass: wafer or LAP fo
- **Ls**
  - thick Al or Cu metallisation
- **Cs**
  - MIM capacitors to 1nF/mm2
  - Pit capacitors > 25nF/mn
- **Rs**
  - TaN, NiCr resistors
  - @ ~ 100Ω/square



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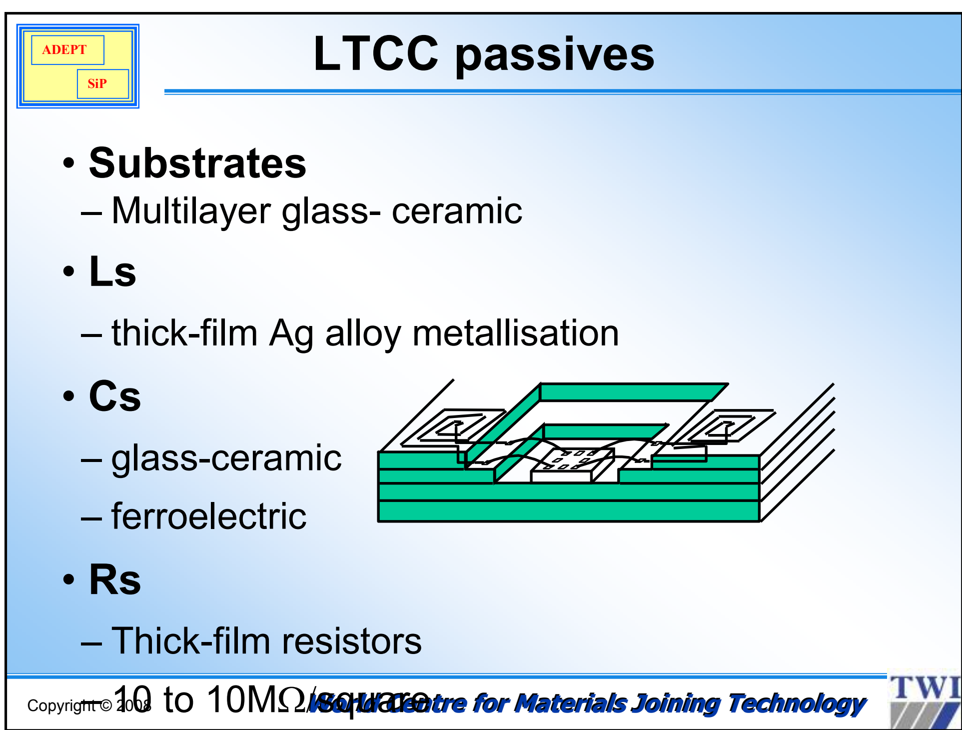
ADEPT
SiP
LTCC passives
• Substrates
– Multilayer glass- ceramic
• Ls
– thick-film Ag alloy metallisation
• Cs
– glass-ceramic
– ferroelectric
• Rs
– Thick-film resistors
– 10 to 10MΩ/square
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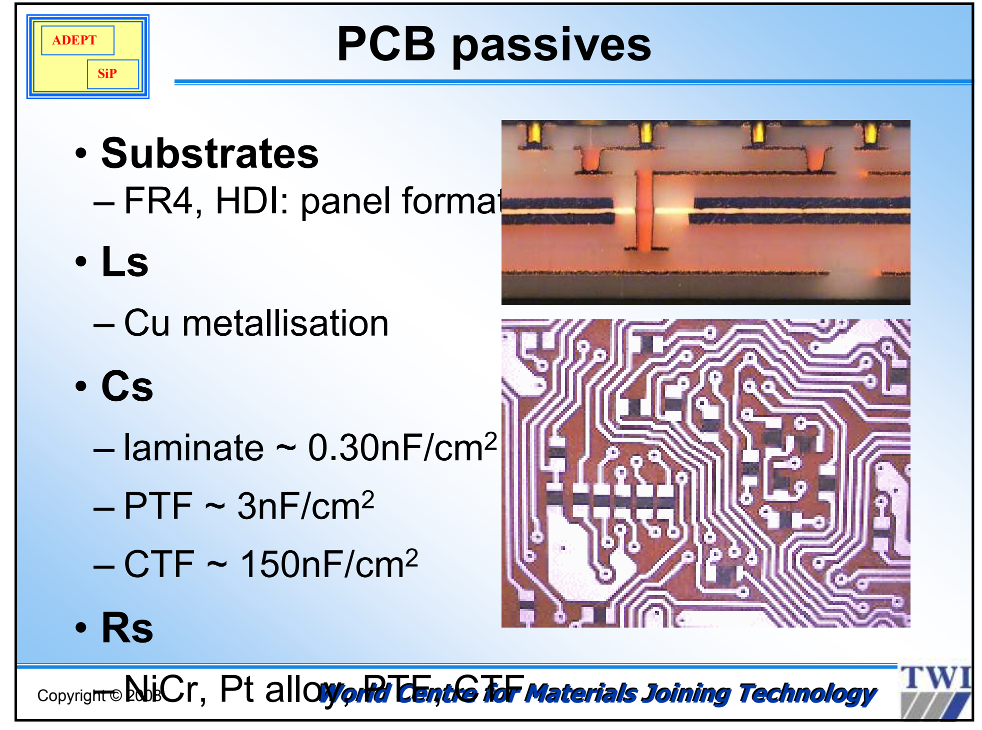
ADEPT
SiP
PCB passives
• Substrates
– FR4, HDI: panel format
• Ls
– Cu metallisation
• Cs
– laminate ~ 0.30nF/cm2
– PTF ~ 3nF/cm2
– CTF ~ 150nF/cm2
• Rs
– NiCr, Pt alloy, PTF, CTF
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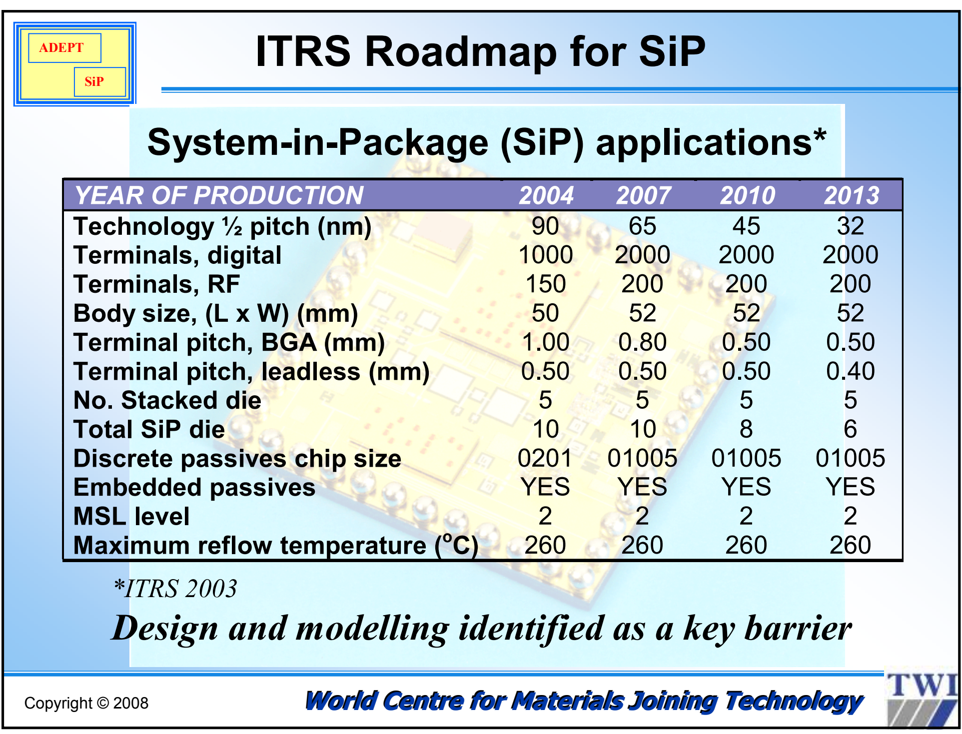
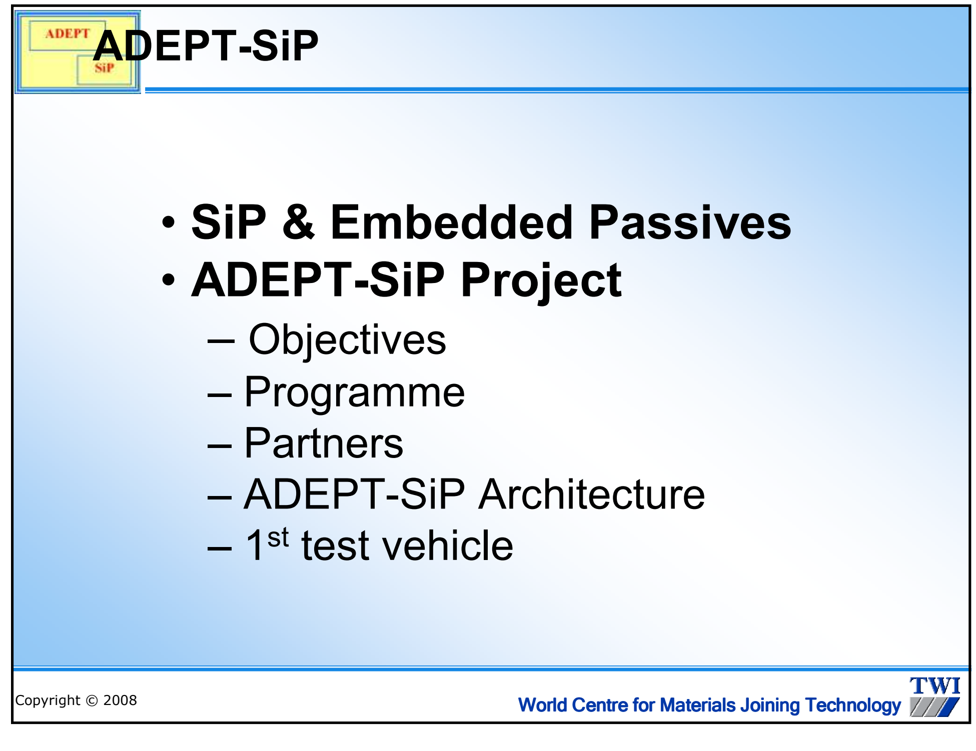


YEAR OF PRODUCTION	2004	2007	2010	2013
Technology ½ pitch (nm)	90	65	45	32
Terminals, digital	1000	2000	2000	2000
Terminals, RF	150	200	200	200
Body size, (L x W) (mm)	50	52	52	52
Terminal pitch, BGA (mm)	1.00	0.80	0.50	0.50
Terminal pitch, leadless (mm)	0.50	0.50	0.50	0.40
No. Stacked die	5	5	5	5
Total SiP die	10	10	8	6
Discrete passives chip size	0201	01005	01005	01005
Embedded passives	YES	YES	YES	YES
MSL level	2	2	2	2
Maximum reflow temperature (^{o}C)	260	260	260	260



ADEPT-SiP

Advanced Design, Partitioning and Test for System-in-Package Electronics (ADEPT-SiP)

- **TSB Technology Programme**
- **May 2006 – April 2009**
- **Design, Modelling & Simulation**
- **Objective:** *To develop and demonstrate a right-first-time design and supply chain management methodology for novel System-in-Package electronic product functions*

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ADEPT-SiP programme

- **Technology definition**
  - **Active device assembly**
  - **Interconnect**
  - **Embedded L,C,R passives**
- **Technology development**
- **Technology characterisation**
  - **RFOW**
- **Design kit generation (PDKs)**
  - **Right-first-time design**
- **Technology demonstration**
  - **RF application**
  - **Digital application**

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Partners & Roles

- **TWI -** assembly, packaging, reliability, environment
- **Filtronic -** SiP & GaAs design, SiP build, end-user
- **Zarlink -** SiP & silicon design, SiP build, end-user
- **Zuken -** design tools development, supply chain
- **AWR -** RF design tools, PDK development
- **QuantumCAD -** substrate & package design
- **Wurth Elektronik -** PCB design & manufacture
- **Flomerics -** thermal & EMC modelling, supply chain
- **Leeds -** design, measurement, models, design kits

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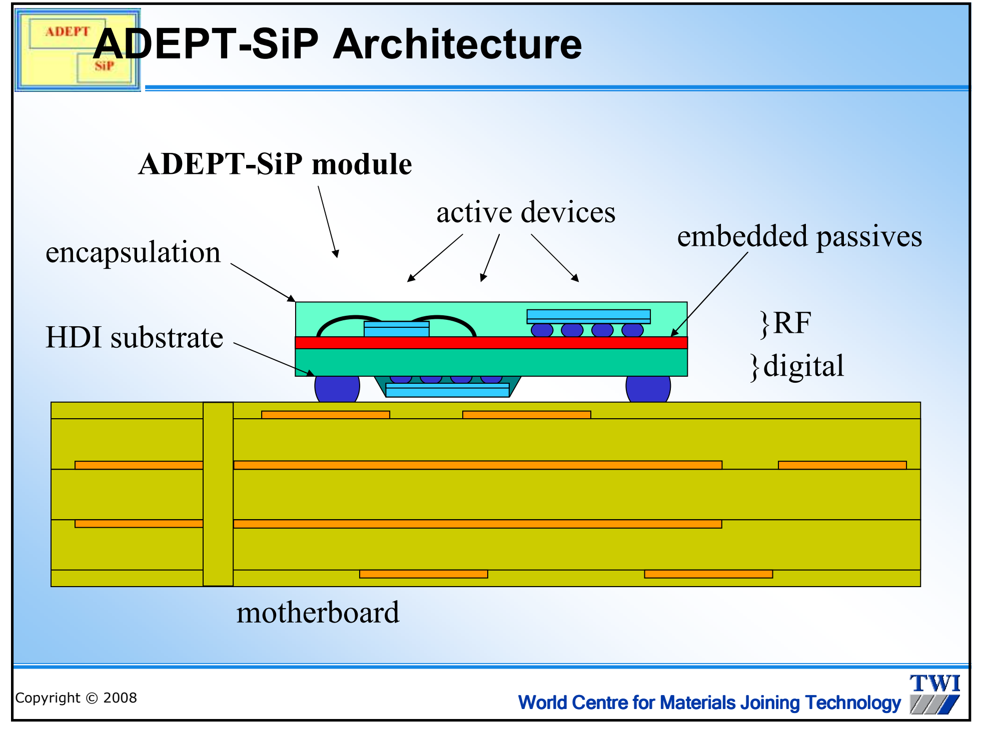
ADEPT-SiP Architecture



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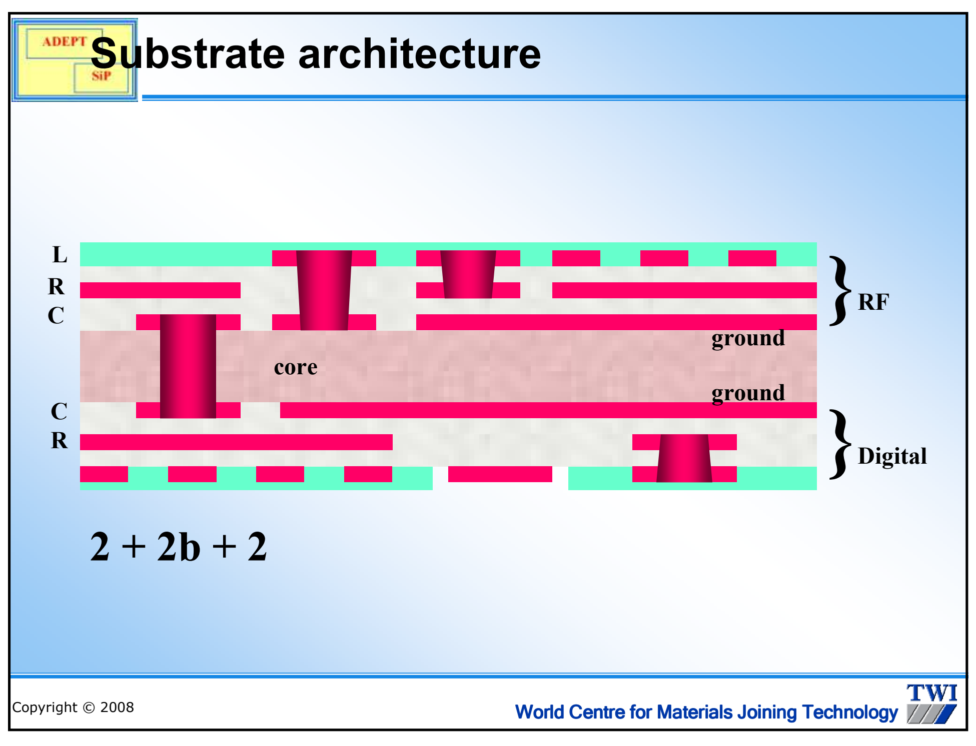
ADEPT
SiP
Substrate architecture
L
R
C
C
R
core
ground
ground
RF
Digital
2 + 2b + 2
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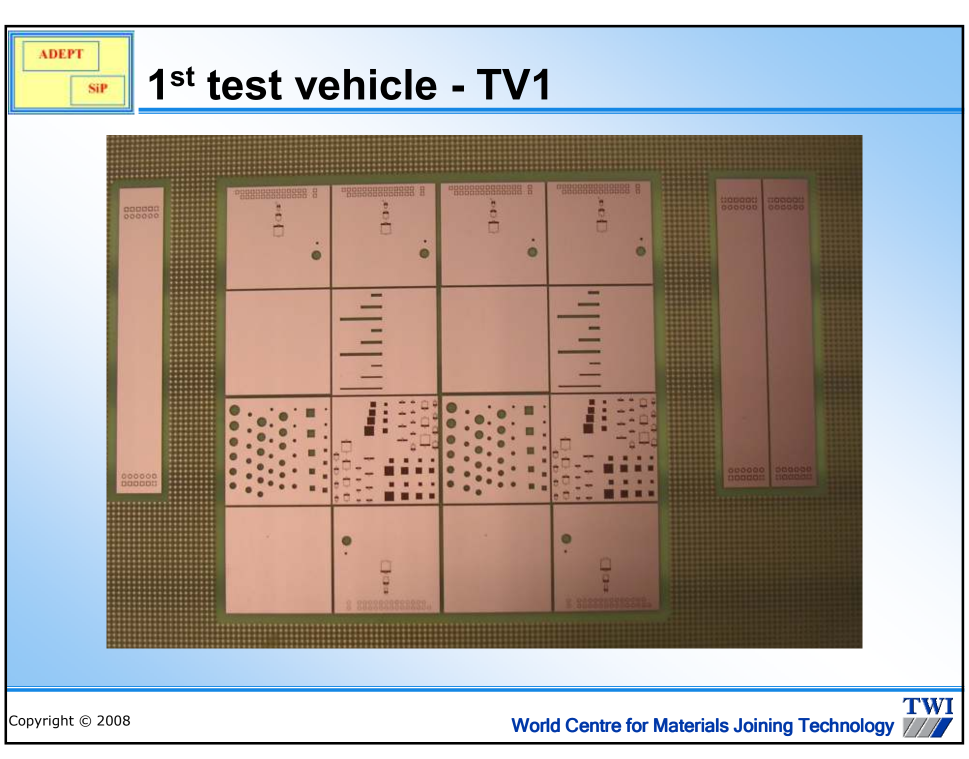
ADEPT
SiP
1st test vehicle - TV1
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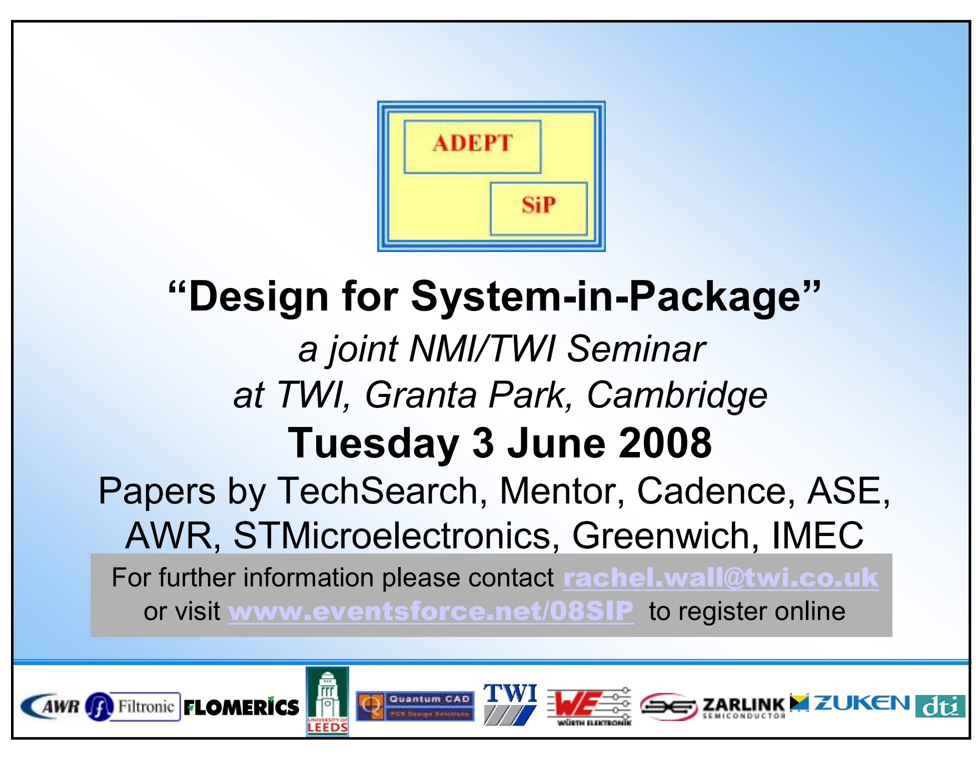
ADEPT
SiP
“Design for System-in-Package”
a joint NMI/TWI Seminar
at TWI, Granta Park, Cambridge
Tuesday 3 June 2008
Papers by TechSearch, Mentor, Cadence, ASE,
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