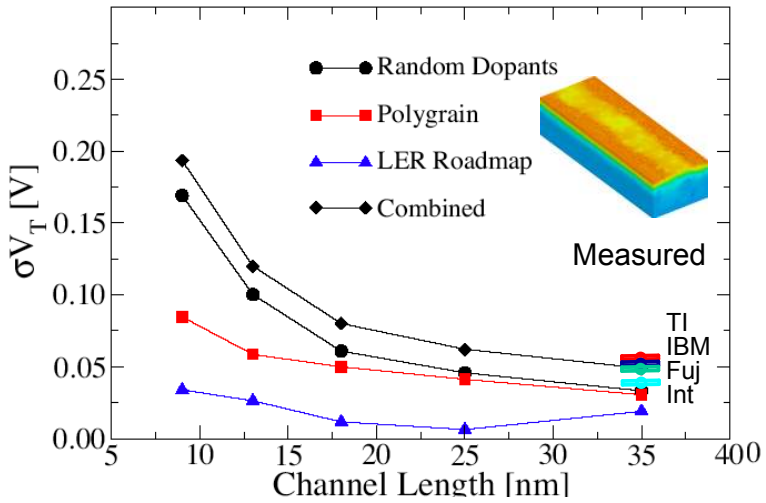
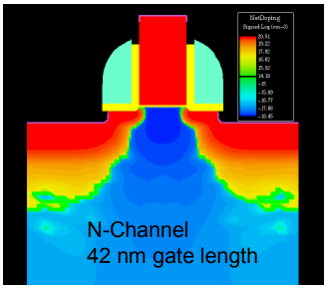
Combined variability in bulk MOSFETs

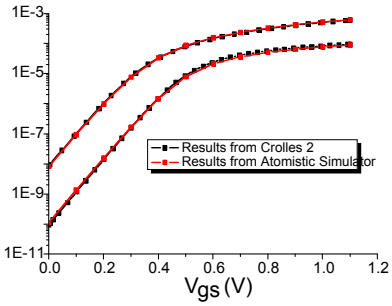
High performance 45nm technology node



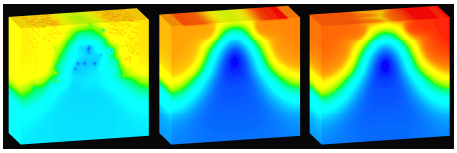
Measured and simulated variability

LP MOSFETs 45nm technology node

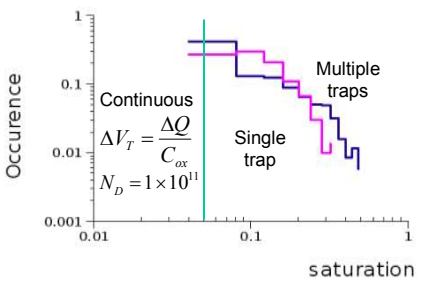


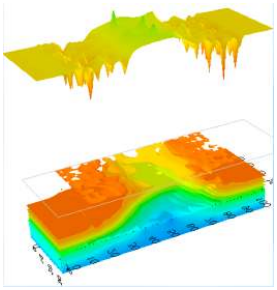


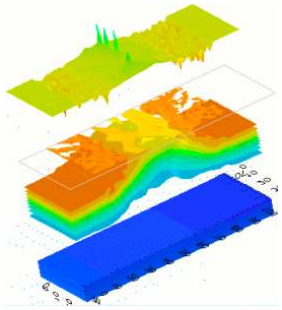
	σV_T (50 mV)	σV_T (1.1 V)
Experiment	62 mV	69 mV
Simulation	62 mV	67 mV

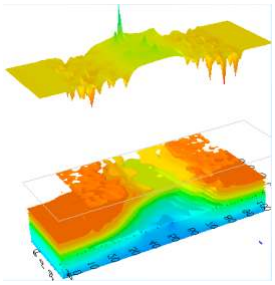


Statistical reliability

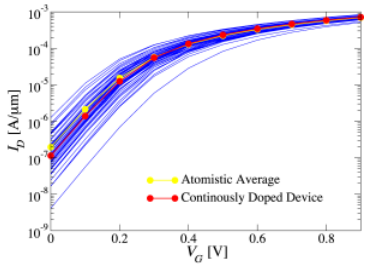


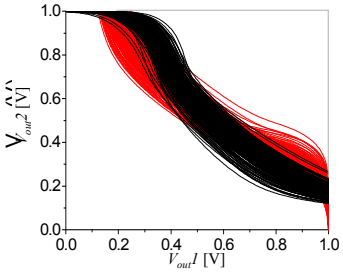


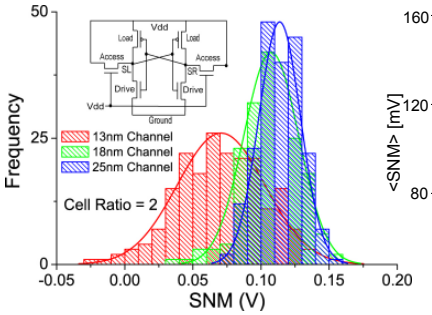


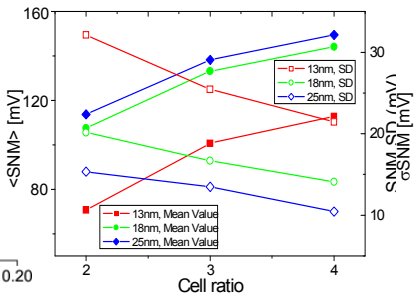


Impact of bulk MOSFET scaling of SRAM

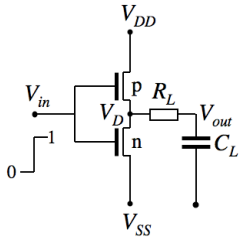


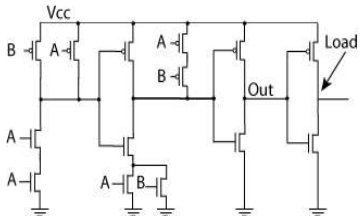


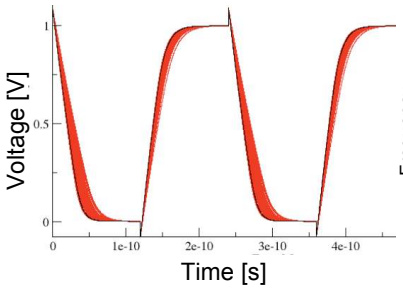


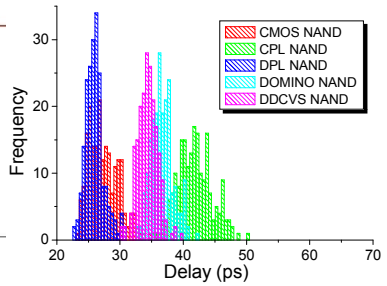


Timing variability

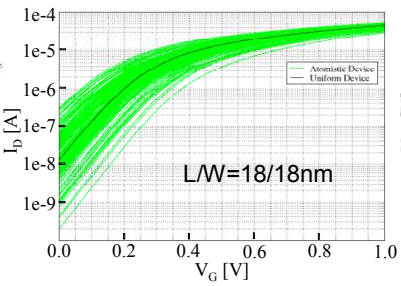


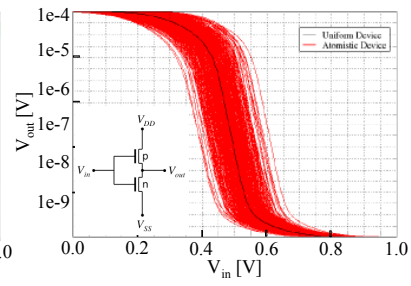


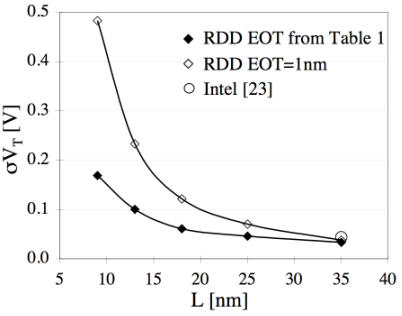


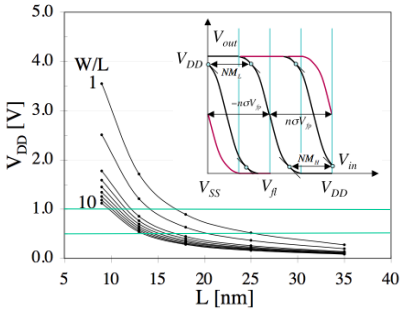


Hard logic faults

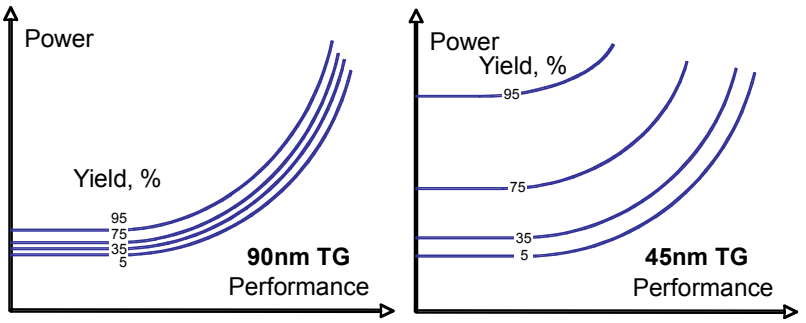




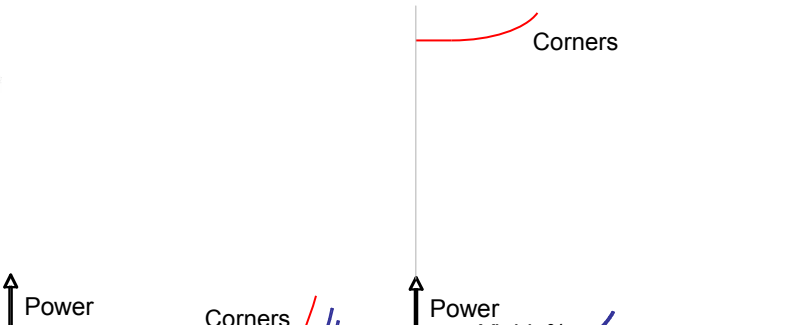




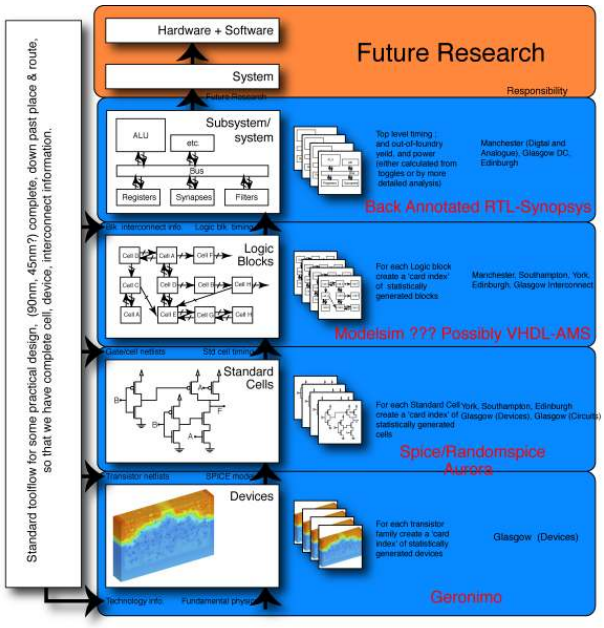
Performance/Power/Yield (PPY) trade-off



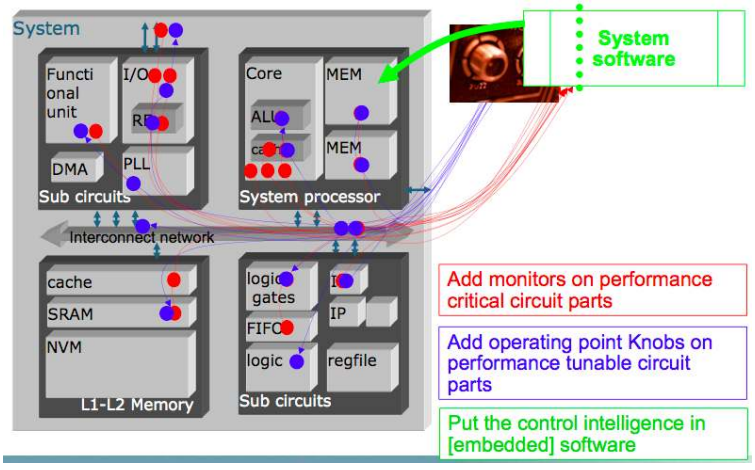
Performance/Power/Yield (PPY) trade-off



NanoCMOS: Grid based statistical simulation

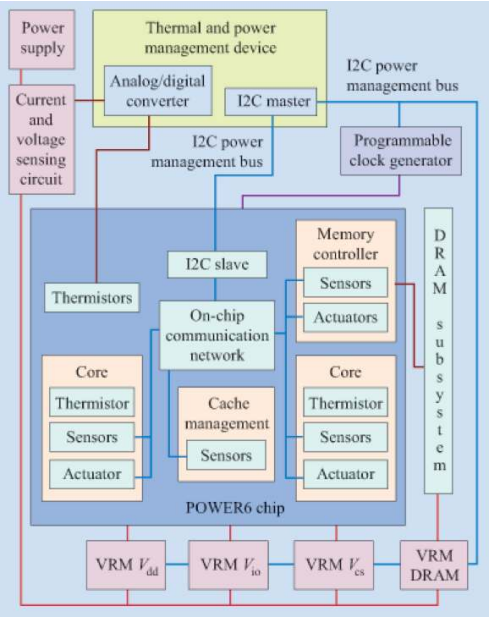


The monitors and knobs approach



The “Technology Aware Design” of IMEC

The Power 6 processor of IBM



CMOS variability research in Europe
ESSDERC/ESSIRC 2008 Workshop

REALITY: Reliable and variability tolerant system on a chip design in More-Moore technologies (EU FP7) B. Dierickx, IMEC

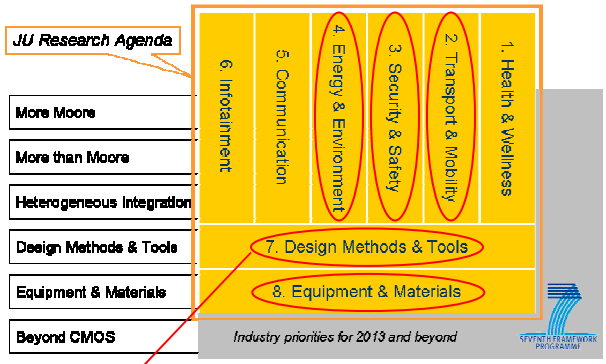
NanoCMOS: Meeting the design challenges of the nano-CMOS electronics (UK EPSRC), A. Asenov, GU

PULLNANO: Pulling the limits of the nano CMOS Electronics (EU FP6), H. Maes

NANOSIL: Silicon-based nanostructures and nanodevices for long term nanoelectronics applications (EU FP7), R. Clerc

NanoMat: Meeting the material challenges of the nano CMOS electronics (UK EPSRC), A. Shluger, UCL

ENIAC JTI First Call



Device, circuit, and system variability and reliability.

Hardware/software model driven hi-level synthesis/flow/reuse/design.

€30M